SYNOPSYS®

Synopsys and AIEC

low power

Features

- Automatic power reduction,
- Fast and accurate pre- and post-synthesis power analysis
- Tight integration within synthesis flow (same database, user commands, user interface, library, etc.)
- Broad library and simulation interface support

Benefits

- Delivers 20 to 60 percent power reduction per synthesizable block
- Enables power-driven tradeoff analysis and early detection of hot spots
- Easy to use, minimal learning curve for existing Design Compiler users

AIEC Slashes IC Power Consumption with Power Compiler™

Many engineers try to keep integrated circuit (IC) power requirements low, but for the design team at Automotive Integrated Electronics Corporation (AIEC), low power consumption is essential. AIEC designs custom ICs for automotive applications. In the harsh environment of an automobile's engine compartment, power management is critical. Without it, the operating temperature of the IC, combined with the ambient temperature of the engine compartment, can swiftly soar above acceptable operating levels.

The IC Design Team made up of Frank Emnett, Rich Gauer and Mark Biegel of AIEC display the positive results enabled by Power Compiler on the Real Time Engine Controller (RTEC™) I/O processor.

To get the specifications for their custom devices, the AIEC design team provides design services to a silicon partner, in this case STMicroelectronics, who sells the chip to the automotive customer. AIEC's designs are a mixture of technologies ranging from mixed-signal to pure digital devices.

"The main functions of the AIEC designs are for engine control and the communications systems on automobiles," says Frank Emnett one of four design engineers on the AIEC team. "In one particular project, we designed a custom set of peripherals for an engine control application that resides in a mixed-signal IC. The chip interfaces to a microprocessor (MPU), in this case a Motorola 68K derivative, to provide highly precise timing and control functions."

For example, the chip tracks the position of an engine based on input signals from the cam shaft and crank shaft in real time and uses that information without any processor intervention to control ignition and injection outputs, generate pulses for the tachometer and control analog to digital conversions. The device also collects timing information on different events in the engine. For instance, it measures feedback signals from the fuel injectors, and through embedded software, determines their temperature and adjusts fuel metering accordingly.

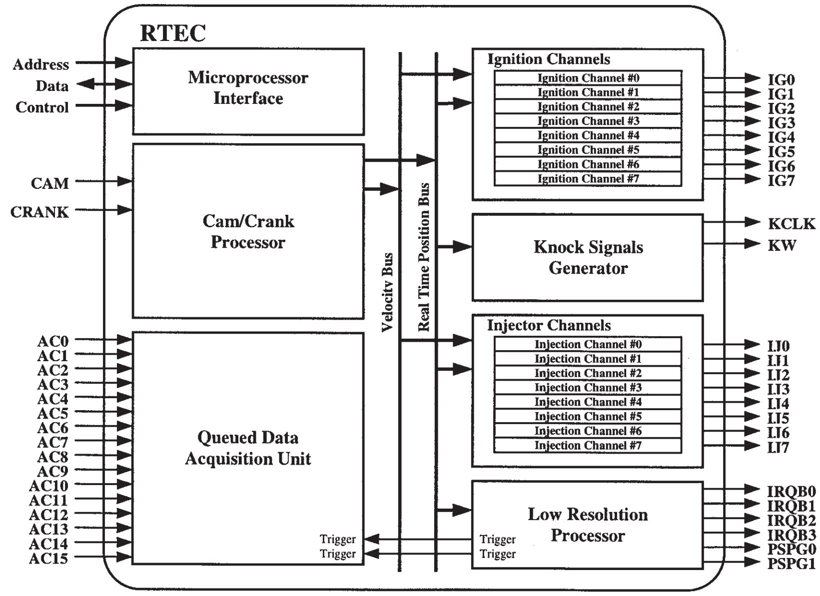
ease-of

"Over the two years of development, the number of features increased significantly as the customer's software group came up with more and more hardware features, resulting in pretty high power consumption and operating temperature when first silicon was manufactured," says Frank Emnett.

"The object of this design was to offload low-level processing from the MPU, so it can be used for the high-level engine control algorithms," Emnett explains. "By monitoring and controlling engine functions, the chip lowers emissions, improves gas mileage and increases engine performance. We also provided the chip with hooks so that it could be used for diagnostic purposes."

The design evolved over time from 50K gates to around 200K gates as the customer's design engineers requested more features. Manufactured in STMicroelectronics' 0.5 micron process, the chip contained a few analog components in addition to the digital logic. It also used seven embedded memories, all dual-ported static RAM. When completed, the chip would be housed in a 128-pin package quad flat pack (QFP) or ball grid array (BGA). The design team used a Verilog synthesis-based design flow. The challenge was to design this semi-custom IC to a constantly expanding range of specifications.

"Over the two years of development, the number of features increased significantly as the customer's software group came up with more and more hardware features," says Emnett, "so the chip was originally specified to be much smaller than it eventually became. Unfortunately the original power budget didn't increase. As a result, we had some pretty high power consumption when first silicon was manufactured and its power and operating temperature were measured."



Block diagram of the Real Time Engine Controller using Power Compiler to minimize power throughout the chip.

"Using Power Compiler's clock gating and some other power management techniques we were able to reduce power from 280mA-300mA range to 80mA range, and that's a figure we can live with," states Emnett.

-use

Emnett points out that this particular chip would reside in a module in the engine compartment, where the ambient thermal temperatures can exceed 125 degrees. In addition, the power supply created its own heat and the temperature rise on the die was a real concern. STMicroelectronics standard libraries are characterized at 125 degrees for automotive and military applications, but the first chip that AIEC designed would end up operating at well above that temperature. In order to stay within the proper power consumption (and heat dissipation) limits, the AIEC team figured that the chip could only consume around 50 to 60 milliamps (mA). The first prototype came in at a 280 to 300 mA, a level far exceeding that necessary for acceptable operating temperatures.

Clearly, the AIEC team had to drastically reduce power consumption. To complicate matters, the customer had already designed the power supply and didn't want to modify it. Costs were also a concern in the price-sensitive, high-volume automotive market, so using expensive heat-dissipating packaging was out of the question. The team turned to Synopsys for a tool to help them achieve the necessary power reduction.

"We've been using Synopsys tools for our designs for some time now," says Emnett. "We use VCS for simulation, Design Compiler™ for synthesis, other tools for clock tree synthesis and so on. We use Cadence's Silicon Ensemble for back-end place and route. Since we had experience with Synopsys' tools, we decided to give Power Compiler a try."

Power Compiler automatically minimizes power consumption at the register transfer (RT)-level and at the gate level. Power Compiler, built on top of Design Compiler, simultaneously optimizes a design for timing, power and area. The tool's push-button power reduction capabilities use clock-gating at the RT-level, and simultaneous optimization for timing, area and power at the gate level. It also provides seamless integration with its links-to-layout methodology.

The AIEC team decided to try the clock gating capabilities of Power Compiler to see what power consumption improvements it could offer. Clock-gating is a common power reduction technique implemented manually in many power critical designs. Power Compiler automates this technique during the design elaboration stage, without requiring any changes to the RT-level source. The potential power savings by clock-gating can be very quickly estimated by Power Compiler, again, without any changes to the source code. Power Compiler gates the clocks of individual synchronous-load-enable register banks instead of circulating the output back to the input when the load enable condition is low.

"I was a little nervous about this technique because we'd never used it before," says Emnett, "but things came out great. We used some other power management techniques along with Power Compiler to further reduce power consumption. For example, we discovered that one port of the dual ported RAM was only used a small percentage of the time, so we powered it down when we didn't need immediate access to the data."

The AIEC team also received some help from STMicroelectronics to reduce the number of end points on a clock tree through use of an integrated clock gating cell designed by the STMicroelectronics library services organization. The team then estimated the power saved both with Power Compiler and the other techniques to see how the next spin of the IC would turn out. Satisfied that an acceptable power reduction had been realized, another chip was manufactured and tested. The results were impressive.

"I was a little nervous about this technique (Power Compiler's clock gating) because we'd never used it before, but things came out great!" said Frank Emnett.

"The power consumption went down to the 80 mA range," Emnett says, "and that's a figure that we can live with. We also reduced the electromagnetic interference (EMI), because we reduced the amount of switching in the circuit. Reducing EMI is also very important in automotive applications, due to its effect on radio noise. We figure that of the total power savings, about two-thirds was due to Power Compiler and one-third was a result of the other techniques. We were very happy with the outcome. We finished on schedule and we drastically reduced power consumption. We'll be using Power Compiler on all of our subsequent designs."

For information related to products, training or support services please visit the Web at www.synopsys.com. For sales assistance, please call 1 650 584 5000.

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