



# The SoC Design Platform and Its Application in the Automotive Industry

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**Synopsis:**

*A system-on-chip (SoC) is generally defined as an Integrated Circuit (IC) that is designed, or customized, for a specific application. SoCs are typically used in embedded systems where the microprocessor core, associated memory, and custom peripheral set are integrated together on a single silicon substrate.*

*To best understand how SoC technology can be applied to the automotive industry, it is beneficial to review how a similar technology (Application Specific Integrated Circuit (ASIC)) has been used to build custom ICs for automotive applications.*

## **A**IIEC Develops SoC Design Platform Based on the ARM966E-S™ Core

Automotive OEMs have traditionally used ASICs to enhance their electronic products offering. These ASICs, or custom chips, are typically designed and integrated into systems to increase performance and provide a differentiating quality through innovative hardware. A good example of an ASIC recently put into production by a major automotive OEM used dedicated hardware to track the position of an engine independently of the microprocessor. This innovative hardware approach eliminated the need for the microprocessor to track the engine thus freeing valuable processor throughput. With the processor relieved of the interrupt intensive I/O tasks, higher-level control algorithms such as model-based control were implemented providing real benefits including increased fuel economy and reduced emissions.

An alternative to the ASIC approach for product differentiation uses off-the-shelf standard products or microcontrollers. These microcontrollers contain dedicated peripherals and, like ASICs, the peripherals are designed to off load the controlling microprocessor. However, unlike an ASIC, the peripherals found within microcontrollers are designed to be "general purpose" such that standard product manufacturers can market a single product across multiple markets and applications. One disadvantage of this standard prod-

uct approach is that the "general purpose" peripherals result in lower performance than that of ASIC peripherals. With an ASIC, the peripherals are designed with a focus on controlling specific tasks and therefore require less processor intervention. This frees the processor of the low level I/O tasks and allows higher-level control algorithms to be implemented for increased system performance. Furthermore, ASIC peripherals achieve high performance by reducing the latencies normally associated with software controlled "general purpose" peripherals. The dedicated hardware found within an ASIC peripheral reduces software overhead, which provides faster response times and thus greater accuracies for the device under control.

Although it is generally accepted that an ASIC provides higher performance than general purpose peripherals found on standard product microcontrollers, the cost of adding a discrete ASIC to the system has often been difficult to justify. Fortunately, with the relentless pursuit of smaller semiconductor geometries, it is not only possible but it has become economical to integrate the ASIC peripherals together with the microprocessor and associated memory into what has become known as a SoC.

In fact, for high volume applications it is more cost effective to use a custom SoC than it is to use a standard product. This is because SoCs can be designed to a smaller die size, and thus lower cost, than

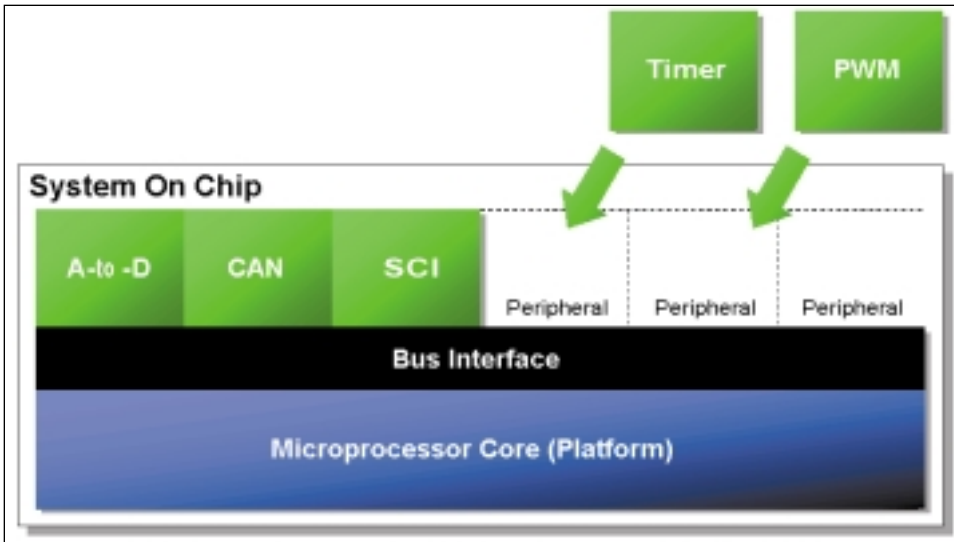


Figure 1: System on Chip Platform Based Design

that of a standard product. For example, a standard product that is designed for many different applications will have a fixed memory size whereas the SoC's memory can be sized for the given application. Since memory typically accounts for more than half of the die size in today's automotive flash technology-based microcontrollers, significant cost savings can be achieved by appropriately sizing the memory of an SoC. Furthermore, a SoC's peripheral set is designed for a specific application that requires less space than a standard product peripheral set, which is designed to accommodate many applications.

A disadvantage of developing a custom SoC is the cost associated with semiconductor tooling. However, with the high volumes associated with automotive applications, SoCs actually become more economical than standard products, which do not have an associated tooling cost. As an example, a typical SoC tooling cost of \$500,000 amortized over a production run of 1 million pieces/year for 5 years equates to \$0.10/device.

Understanding that SoCs designed for a specific application can be made smaller than a standard product, the tooling cost are easily justified through the savings in silicon cost alone. Additional value comes with increased performance and product differentiation made available by SoCs.

Although SoCs provide for higher system performance at a lower cost than that of standard products, one obstacle to the proliferation of SoCs into the automotive industry has been with the complexity associated with developing a SoC. Furthermore, schedules and budgets have a tendency to slip with custom chip developments while the ever-present bugs associated with new designs tend to raise overall risk.

However, with the advent of SoC platform-based design, many of the common problems associated with custom IC design are eliminated or at least reduced to manageable levels. First, platform-based design uses a building block approach where each block is a predefined functional unit that requires no new development. Each block has been, in essence, pre-qualified and known to operate correctly in a system, which mitigates the risks associated with bugs commonly found in new designs. Second, platform-based design becomes an exercise in the integration of the pre-defined building blocks. This process of integration is well understood such that schedules, budgets, and risk can be controlled.

The primary building block of SoC based design is the microprocessor core. The core provides the foundation or platform from which to build the SoC and for this reason, it is important to choose a widely accepted microprocessor core that is well established and broadly supported. For exactly these reasons, AIEC has chosen to build its first SoC development platform around the ARM966E-S CPU core. The ARM966E-S core is part of the ARM family of microprocessor products, which have become the most widely accepted embedded RISC processors in the world. More than 100 semiconductor and systems companies have licensed ARM cores making ARM the industry's leading provider of 16/32-bit embedded RISC microprocessors. In becoming a de-facto standard of high-performance, low-cost microprocessor cores, the ARM cores are broadly supported from many aspects including development tools, real time operating systems, and application software.

AIEC's first development platform is targeted specifically towards automotive embedded control applications such as powertrain, anti-lock braking, and air-bag systems. The microprocessor core used for this platform is the AIEC9, which is based on the ARM966E-S CPU.

The AIEC9 microprocessor core forms the cornerstone of the development platform and provides the highest performance microprocessor core built to date utilizing embedded flash technology running over

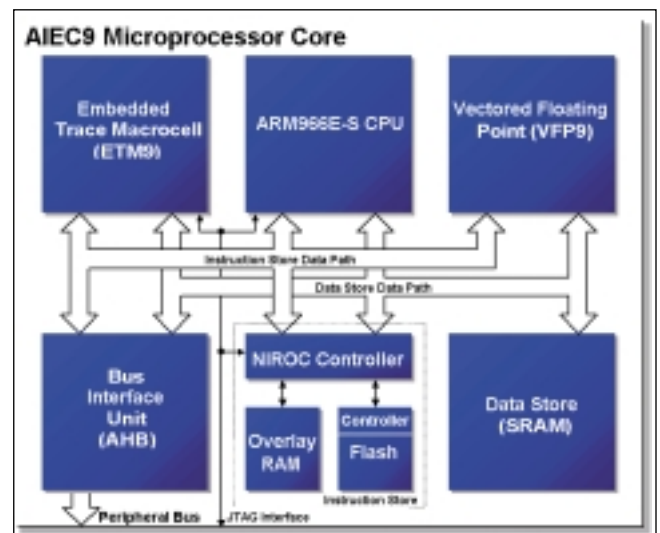


Figure 2: AIEC9 Microprocessor Core



the extended automotive temperature range (-40°C to 125°C). The high-performance of the AIEC9 is in part due to the memory architecture, which has been optimized for real time control systems where deterministic performance is achieved through execution of instructions directly from flash. An interleaved flash controller allows zero wait state execution of sequential code even with comparatively slow flash. This memory architecture provides the highest degree of deterministic performance while system cost is reduced through elimination of a cache and associated cache controller. Additionally, the instruction store and data store memory sizes can be adjusted for optimal balance of cost and capacity. The memory architecture also supports modification of calibration tables stored in flash through the Non-Intrusive RAM Overlay Calibration (NIROC) circuit. Calibration tables are modified via the JTAG interface completely independent of the ARM966E-S CPU, leaving operation of a system under calibration completely unaltered from production operating conditions. A Vector Floating Point unit (VFP9™) is contained within the AIEC9 to accommodate high-performance floating-point algorithms, which enables the use of automatic code generation tools for model based system control methodologies. The AIEC9 also contains an Embedded Trace Macrocell (ETM9™) that allows true, real-time software debug of embedded control systems where halting the processor to observe data and program flow is not possible. Finally, the AIEC9 uses the industry standard AMBA® Advanced High-performance Bus (AHB) for interfacing to peripherals.

In addition to the microprocessor core, the peripherals are a key factor to SoC based platform design. Again, the idea is to use a building block approach whereas designs can be rapidly assembled using pre-qualified, known working functional blocks. This approach tends to reduce overall design risk while at the same time it facilitates reuse of existing software drivers.

Generally, a set of pre-designed peripherals will include application specific peripherals, communication peripherals, and general purpose peripherals.

Application specific peripherals are designed to control a particular application and provide the highest levels of performance. The high level of performance is a result of dedicated hardware that is designed to specifically control the task at hand while minimizing software interaction. This means that the latency normally associated with interrupts and software control is reduced allowing a quicker response for precision control. For example, a circuit designed to track an engine can respond immediately to a cam or crank shaft input signal where the introduction of software control results in certain latencies or inaccuracies. Communication peripherals usually encompass the standard automotive protocols including SPI, I2C, SCI, J1850, and CAN. Here again, using pre-qualified peripherals can significantly reduce hardware development time while the re-use of drivers reduces software development time. General purpose peripherals add a certain amount of flexibility to the system since they can be used for a variety of in-system applications while being controlled through software.

Given the pre-defined building blocks including the microprocessor core and peripherals, the complexities associated with developing a custom chip are significantly reduced and thus the risks associated with new product development are reduced. Reducing risk can be taken a step further if the intended SoC is prototyped and tested in the actual system being developed before committing to silicon manufacturing.

To facilitate prototyping SoCs based on the AIEC9 microprocessor core, AIEC provides a development board, the AIEC9DVB, which includes a microprocessor core, associated memory, digital peripherals, and an analog to digital converter. By providing these functions, the AIEC9DVB allows SoCs to be completely prototyped before committing to silicon and the associated tooling cost. Customization of the prototype SoC is accomplished through a Field Programmable Gate Array (FPGA), which

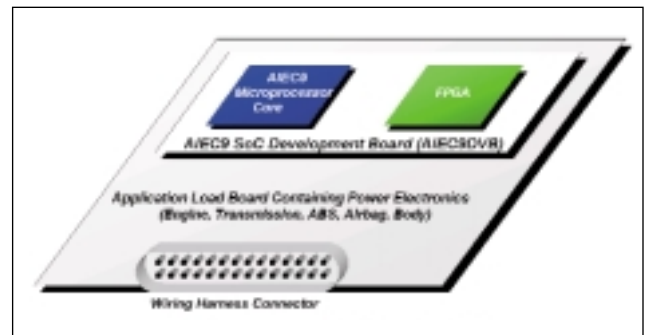


Figure 3: AIEC9 Development Board

allows the user to exactly specify, and pre-verify, the peripherals required for a given application.

Most importantly, the AIEC9DVB provides a prototype environment where system level architecture can be refined through co-design of the hardware and software. Hardware and software components can be readily added to the system and quickly verified using the actual application running in real time. The AIEC9DVB allows the software and hardware teams to work concurrently throughout the design cycle to minimize development times for reduced time to market while improving product performance.

With the advent of SoC design platforms, SoCs will begin to proliferate throughout automotive applications. When compared to off-the-shelf standard products, SoCs have the potential for significantly reducing cost while at the same time improving system performance. The overall risk associated with custom chip development is reduced by using a building block approach while the system can be completely prototyped using an "at speed" development platform. The development platform emulates the production intent SoC and allows the system level architecture to be refined through co-design of the hardware and software. Modifications to the hardware becomes as simple as reconfiguring the FPGA. Upon completion of the design, the development platform can be used for continued software development while the silicon is being fabricated.

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