

# Serial Communications Interface (SCI)

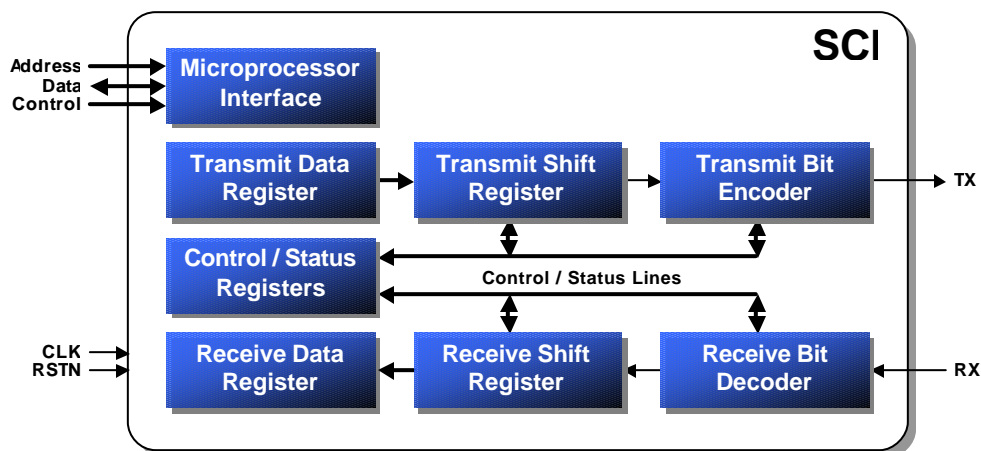
## Product Overview

The Serial Communications Interface (SCI) is an asynchronous full duplex serial communication interface that uses standard Non-Return to Zero (NRZ) data formatting. The data format includes a single start bit, either 8 or 9 data bits, and a single stop bit. The last data bit can be programmed as either an odd or even parity bit. When enabled, parity is automatically generated by the transmitter and checked by the receiver. Parity errors detected by the receiver are indicated with the parity error flag. The SCI contains an internal baud rate generator that provides 8191 different bit rates for matching the system clock rate to the desired transmission frequency. The SCI's transmitter is capable of generating queued idle characters that can be used to wake other nodes or assure adequate time between transmissions for slow reacting nodes. The SCI's receiver samples each data bit 3 times and uses majority voting logic to enhance noise immunity. Data integrity is further assured with the receiver resynchronizing at each falling edge of a bus transition. As a result, discrepancies between clock frequencies of the transmitting and receiving nodes are less likely to cause reception errors. The SCI's receiver can be put to sleep by the controlling microprocessor (uP) once it has been determined that the message is not of concern. The uP will not be burdened with any further interrupts until the receiver recognizes that the unimportant message has completed.

The SCI peripheral is part of AIEC's modular library of components. The SCI can be integrated with other peripherals as part of an ASIC, or it can be integrated with a microprocessor core and associated memory as part of a complete System on Chip (SoC).

## Features

- Full Duplex Operation with Simultaneous Transmit and Receive (Individual Transmit and Receive Enable Bits)
- Standard NRZ Data Format with Single Start and Stop Bits
- Enhanced Noise Immunity Through Majority Voting Logic of Over Sampled Receive Data
- Receiver Resynchronizes on Every Falling Edge for Proper Data Alignment and Improved Reliability
- Programmable Word Length (8 or 9 Bit) with Automatic Parity Generation and Checking
- Advanced Error Detection Includes Framing Error Detect, Noise Detect, Parity Error, and Receive Data Register Overrun
- Transmitter Supports Polled or Interrupt Driven Control with Transmit Data Register Empty and Transmit Complete Flags
- Receiver Supports Polled or Interrupt Driven Control with Receive Data Register Full and Receiver Active Flags
- Both Transmit Data Register and Receive Data Register are Double Buffered
- Receiver Can Be Put to Sleep for Remainder of Unwanted Message and Re-awaken on Either Idle Line Detect or Address Mark
- Transmission of Break Code and Received Break Code Detect
- 8191 Programmable Baud Rates from 64Bits/Sec to 524KBits/Sec Using 16.78MHz Clock



**Serial Communications Interface Block Diagram**

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