

## SAE J1850 Protocol Controller - Variable Pulse Width Modulated, Message Level Interface (J1850VM)

### Product Overview

The J1850VM fully supports the *SAE Recommended Standard J1850 Class B Data Communication Network Interface* for both single byte and consolidated headers using Variable Pulse Width (VPW) modulated bit encoding.

The J1850VM automatically handles the protocol details including message buffering, arbitration, frame delimiters, error detection, and cyclical redundancy generation and checking.

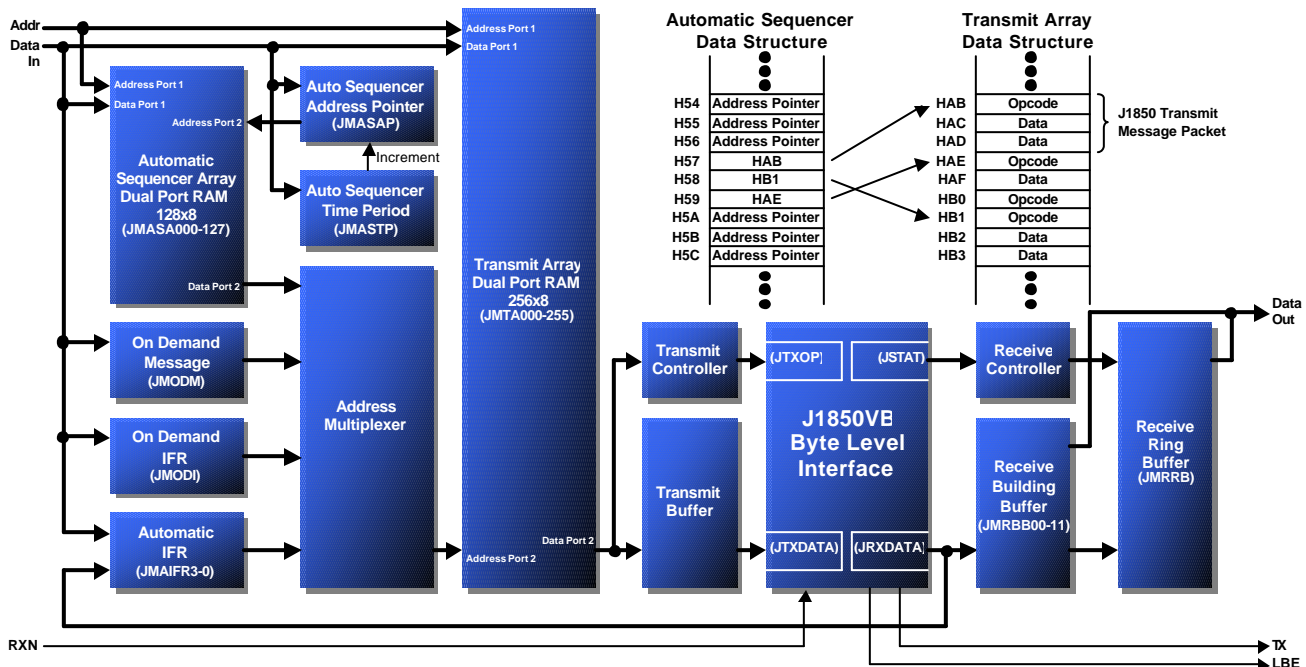
The J1850VM is the most intelligent family member of multiplexing ICs offered by AIEC. Microprocessor intervention is minimized through the use of multiple message buffering. Complete messages are constructed within the Transmit Array and then sent out by the Automatic Sequencer at programmable intervals. Unwanted received messages are filtered out and received messages requiring an In-Frame Response are automatically handled and requires no microprocessor intervention.

Other family members have been optimized for reduced cost where microprocessor throughput is not as critical (see AIEC's J1850VB Data Sheet).

The J1850VM peripheral is part of AIEC's modular library of components. The J1850VM can be integrated with other peripherals as part of an ASIC, or it can be integrated with a microprocessor core and associated memory as part of a complete System on Chip (SoC).

### Features

- *Zero Interrupt Burden Requires No Microprocessor Intervention for Transmitted Messages*
- *Single Byte Header Filtering Completely Eliminates Microprocessor Interrupts from Unwanted Messages*
- *Automatically Responds Using In-Frame Response without Microprocessor Intervention*
- *Complete Arbitration Using Carrier Sense Multiple Access Non-Destructive Contention Resolution*
- *Automatic Re-Transmit on Lost Arbitration for IFR Type 2*
- *Automatic Cyclic Redundancy Check (CRC) and Generation*
- *Error Detection Including CRC Error, Invalid Bit Detection, Invalid Frame Detection, and Frame Length Error*
- *Break Symbol Detection and Generation Logic*
- *Fail Safe Design Prevents J1850 Bus Lock-Up Due to System Errors*
- *No External Oscillator Required (J1850 Bus Timing Derived from Microprocessor Clock)*
- *Interfaces Directly to Industry Standard Bus Transceivers with Programmable Loop Back Delay from 0uS to 31uS and External Loop Back Enable (LBE) Support*
- *Internal Loop Back Mode for In System Diagnostics*
- *Programmable 4x Transmit/Receive Speed*



**SAE J1850 Protocol Controller, VPW Modulated, Message Level Interface Block Diagram**

Automotive Integrated Electronics Corporation (AIEC)  
9034 N. 23<sup>rd</sup> Avenue Suite 13  
Phoenix, AZ 85021  
Phone: (602) 943-7499 Facsimile: (602) 861-1777  
Email: [sales@aiec.com](mailto:sales@aiec.com) <http://www.aiec.com>

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