ARM Processor Interrupt Controller (APIC)

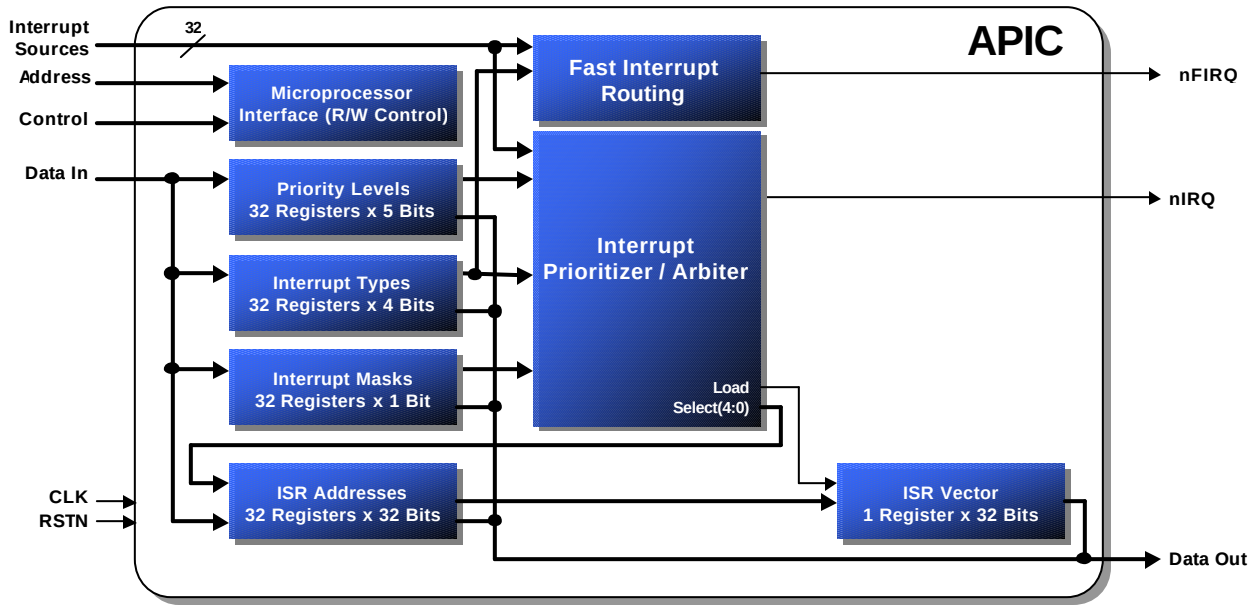
Product Overview

The ARM Processor Interrupt Controller (APIC) prioritizes and submits interrupt requests to the microprocessor for servicing. The APIC is compatible with ARM7TDMI and ARM9TDMI microprocessor cores and allows expansion of ARM's two interrupt sources to thirty-two interrupt sources with extremely low software overhead. One interrupt source can be routed to the ARM's nFIRQ line for an extremely low latency interrupt source. Each interrupt source can be configured as a software or hardware interrupt. Each hardware interrupt source can be active high or active low, and can be level-sensitive or edge-sensitive. The APIC supports thirty-two levels of priority, allowing each regular interrupt source to have its own priority level. Even if all interrupts are programmed to the same priority, a round-robin arbitration scheme ensures that all interrupt sources are serviced and that none are starved. Each interrupt source may be programmed with its own interrupt service routine (ISR) address. The hardware interrupt vectoring feature causes the address of the ISR for the highest priority active interrupt to appear in an APIC register, where it can be fetched by the microprocessor directly from its interrupt vector instruction, ensuring the lowest possible latency.

The APIC peripheral is part of AIEC's modular library of components. The APIC can be integrated with other peripherals as part of an ASIC, or it can be integrated with a microprocessor core and associated memory as part of a complete System on Chip (SoC).

Features

- *Compatible with ARM7TDMI and ARM9TDMI microprocessor cores*
- *Supports thirty-two interrupt sources for the nIRQ interrupt*
- *Any interrupt source can be routed to the nFIRQ interrupt*
- *Hardware interrupt vectoring reduces interrupt service routine latency*
- *Full hardware prioritization of interrupt sources*
- *Interrupts of lower priority levels automatically masked while interrupt is serviced*
- *Round-robin arbitration for interrupts at the same priority level ensures starvation-free operation under the heaviest of loading conditions*
- *Interrupt sources programmable with unique interrupt service routine addresses*
- *Thirty-two priority levels, programmable for each interrupt source*
- *Interrupts can have either a software or hardware source. Hardware interrupts can be active high or low, and edge or level-sensitive*
- *Masking programmable on a per-interrupt source basis*



ARM Processor Interrupt Controller Block Diagram

Automotive Integrated Electronics Corporation (AIEC)
9034 N. 23rd Avenue Suite 13
Phoenix, AZ 85021
Phone: (602) 943-7499 Facsimile: (602) 861-1777
Email: sales@aiec.com http://www.aiec.com