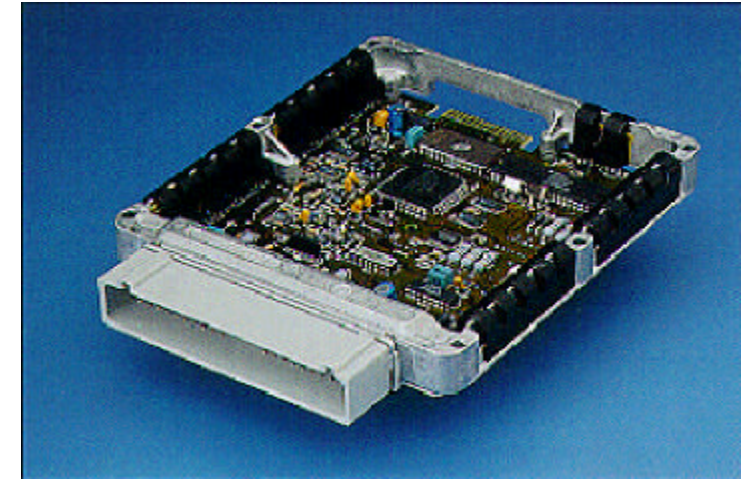

ARM Automotive Conference 2001



Automotive Integrated Electronics Corporation Providing System On Chip Solutions for the Automotive Industry



December 5, 2001

Presentation Overview

- **Automotive Integrated Electronics Corporation (AIEC) Company Background**
- **AIEC's Products and Services (Design Capabilities)**
- **Automotive Application Specific System On Chip (SoC)**
- **SoC Microprocessor Core (ARM9 CPU)**
- **SoC Peripherals**
- **SoC Development Platform**

Automotive Integrated Electronics Corporation

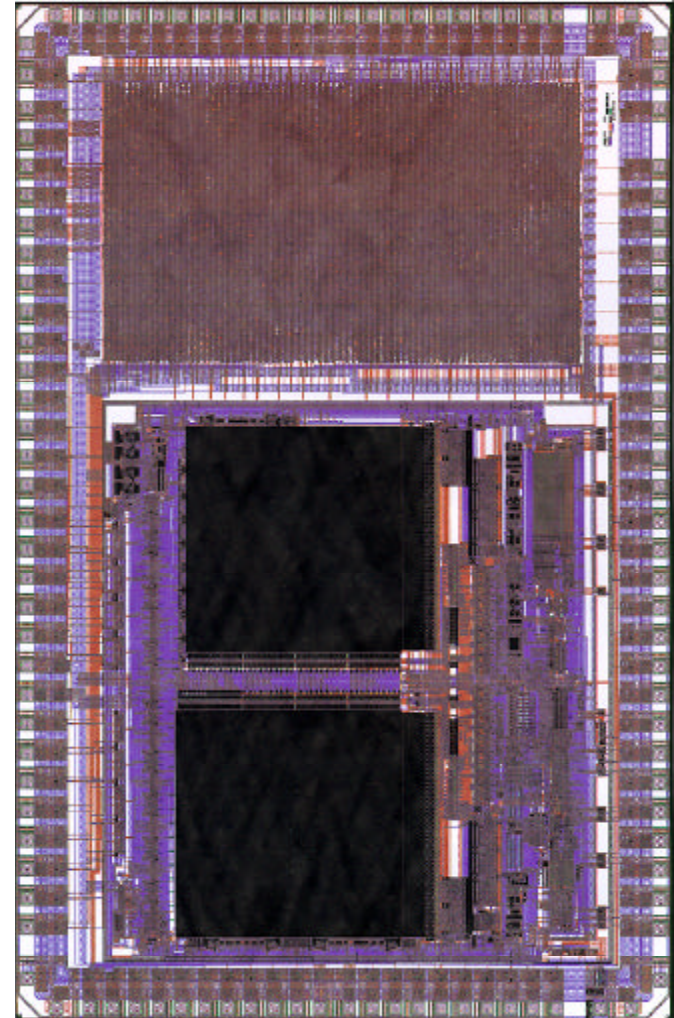
Designing Application Specific Integrated Circuits (ASIC) and Application Specific Standard Products (ASSP) for the Automotive Industry

Designing Integrated Circuits Since 1992, Completed Over 20 ASIC Designs, Several High Volume Production Designs, Some Reaching 5 Million Units / Year

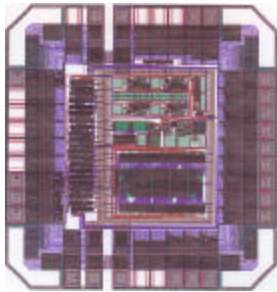
Comprehensive Quality Plan Using QS-9000 Advance Product Quality Planning (APQP), Design Failure Mode and Effects Analysis (DFMEA), 99% Fault Grading, IDDQ Testing

Primary Goal - Differentiate Customer's Products over Competition with Increased Performance at Reduced Cost

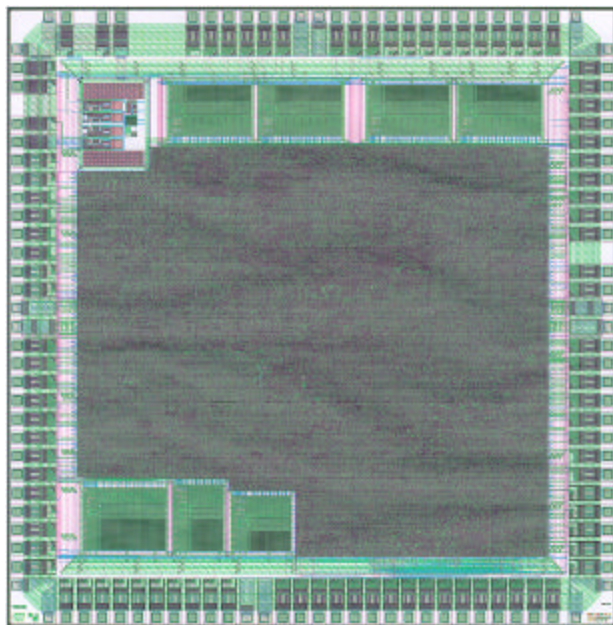
Clear Understanding That Our Success Depends on Our Customer's Success



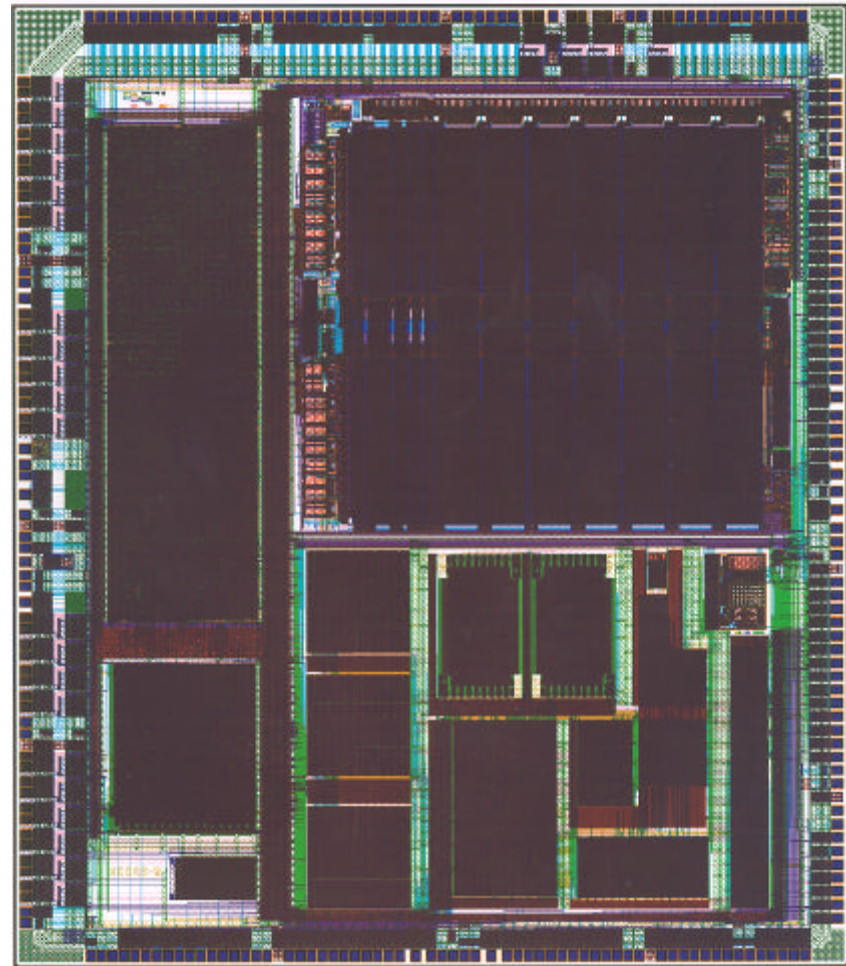
AIEC's Integrated Circuit Design Capabilities



Mixed Signal ASIC
(Airbag Diagnostics)

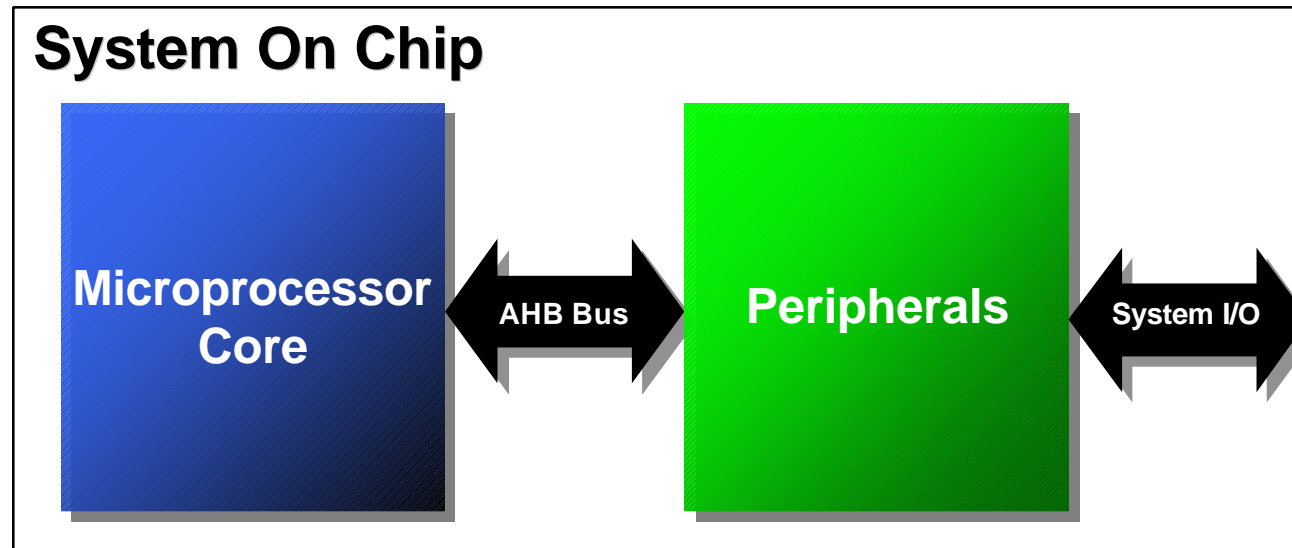


Digital ASIC
(Engine Controller)



System On Chip
(Transmission Controller)

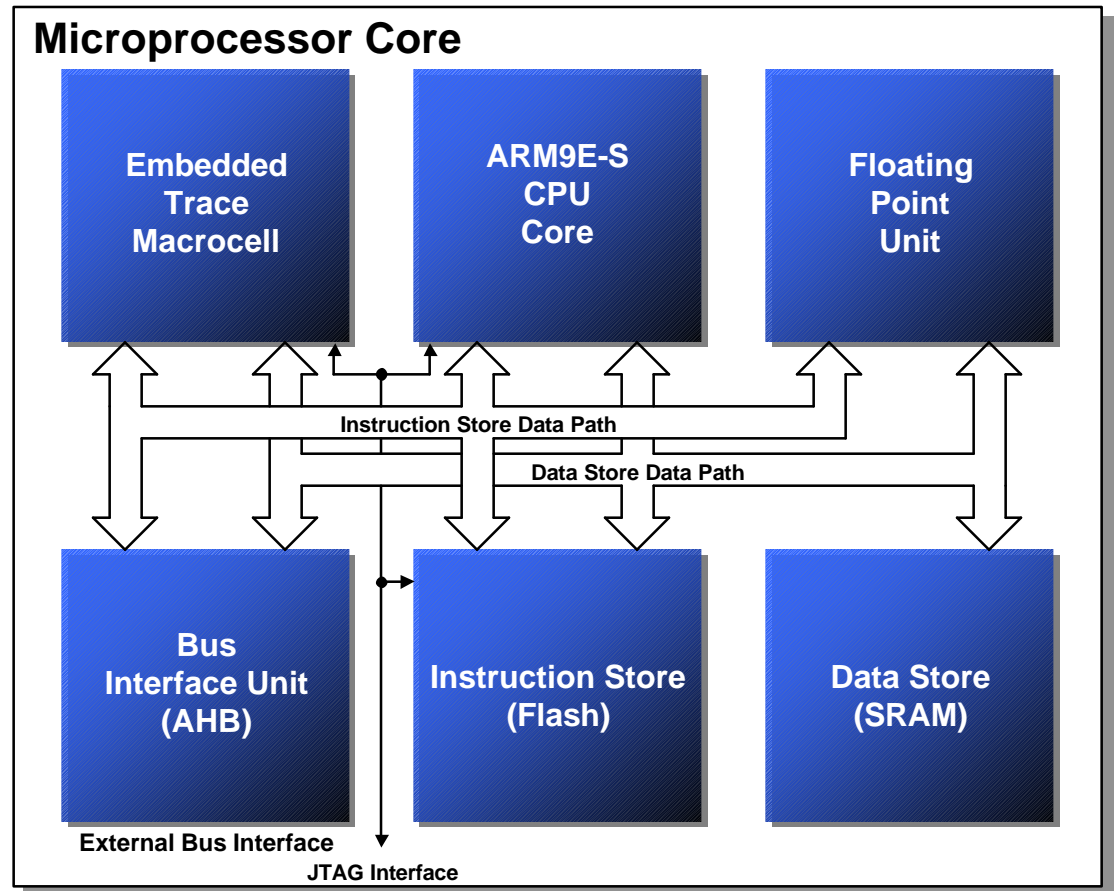
Simplified System On Chip (SoC) Block Diagram



- **Automotive Specific Microprocessor Cores (ARM7, ARM9, ARM10)**
 - Optimized for Real Time Control
 - Memory Architectures Optimized for Cost
- **Automotive Specific Peripherals**
 - Mixed Signal (A-to-D, PLL)
 - Communication (CAN, J1850, SCI, SPI)
 - Application Specific (Real Time Engine Controller)
 - Customer Specific (Customer Intellectual Property)

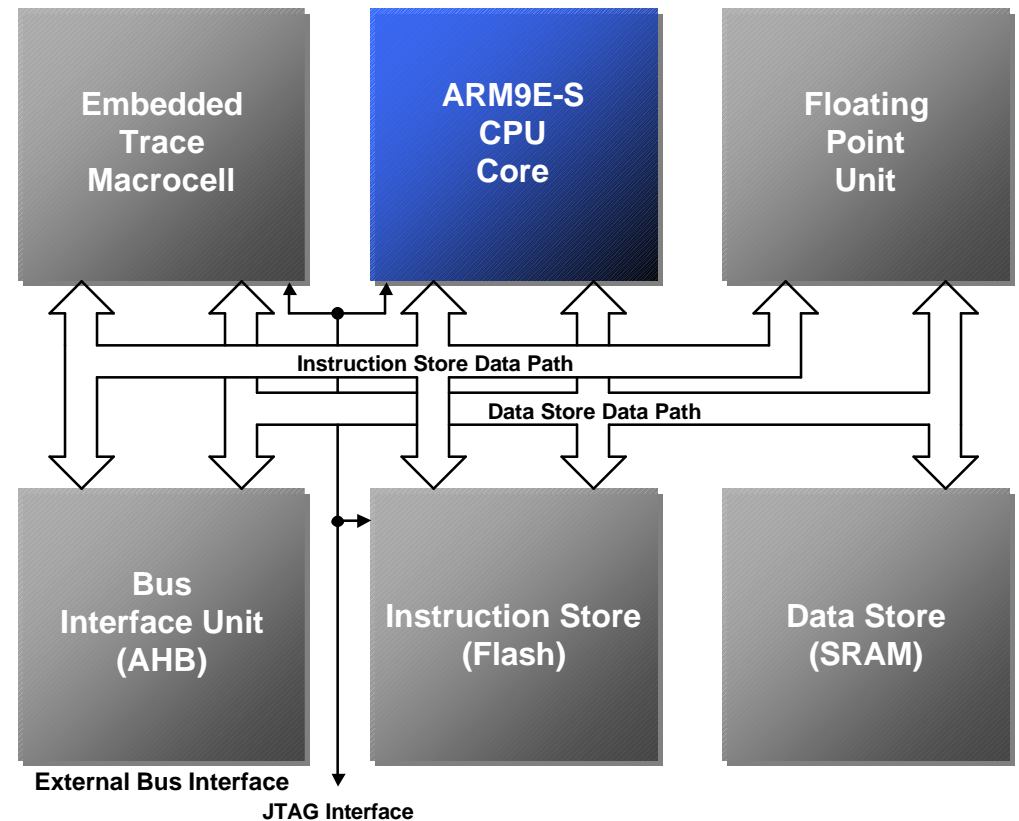
System On Chip Microprocessor Core

- ARM9E-S
- Instruction Store
- Data Store
- Floating Point Unit
- Embedded Trace Macrocell
- AHB Interface



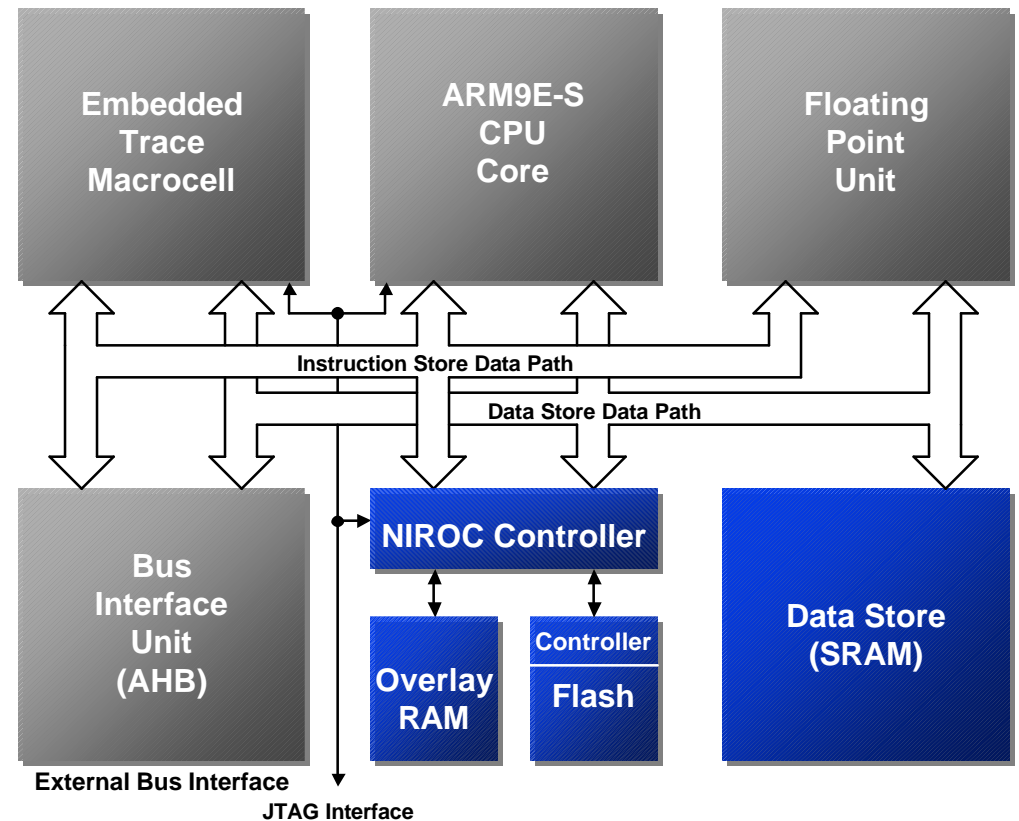
ARM9E-S CPU Core

- 32-Bit RISC CPU Core
- Code Compression On-The-Fly (Thumb Instruction Set Compatible)
- Embedded ICE with JTAG Software Debug Facilities
- DSP Extensions to Instruction Set Includes Single Cycle MAC and Saturating Arithmetic



Memory Architecture

- Data Store Uses Static RAM (Size User Configurable)
- Instruction Store Uses Flash (Size User Configurable)
- Instruction Memory Controller Pipelines Instructions to Allow Inline Code Execution at Processor Clock Speed (>100MHz)
- Calibration Fully Supported Through Non-Intrusive RAM Overlay Calibration (NIROC)



Non-Intrusive RAM Overlay Calibration (NIROC)

•Equivalent to NEXUS Class 4

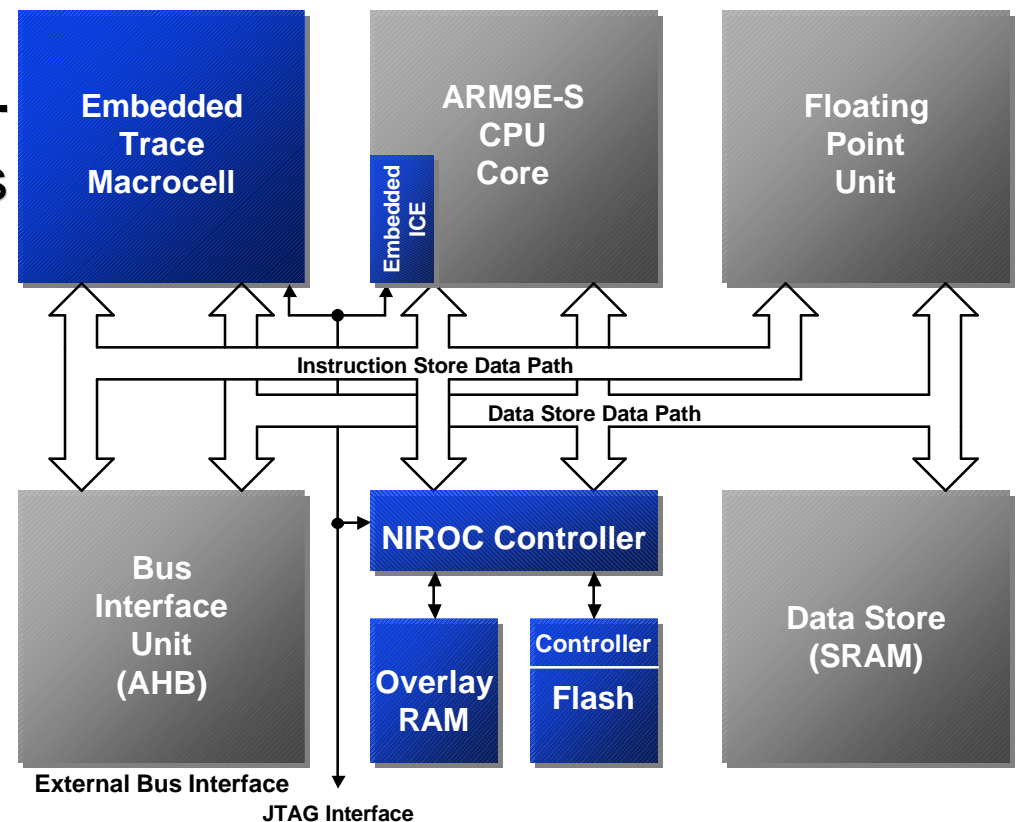
- Static Development Features
 - ✓Breakpoints, Single Step, etc.
- Dynamic Development Features
 - ✓Monitor Program Flow
 - ✓Modify Memory

•Calibration Support (NIROC)

- Monitor Control Variables
- Memory Substitution

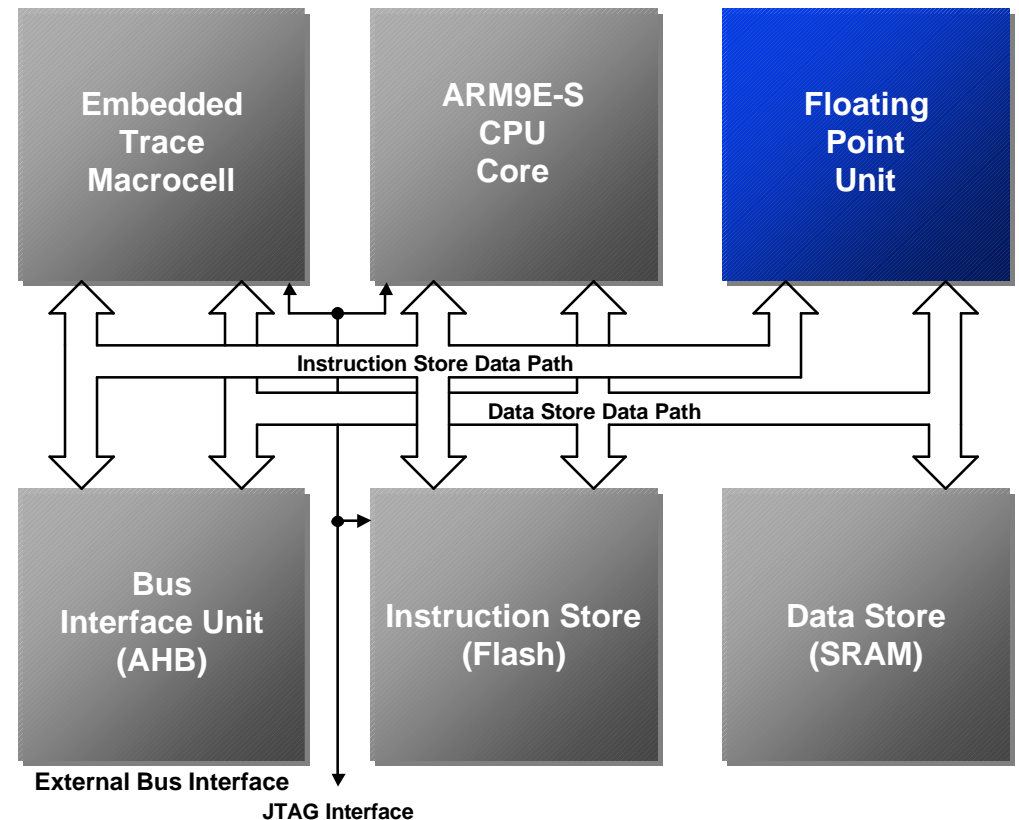
•Algorithm Development

- Rapid Prototype Controller,
Hardware In the Loop



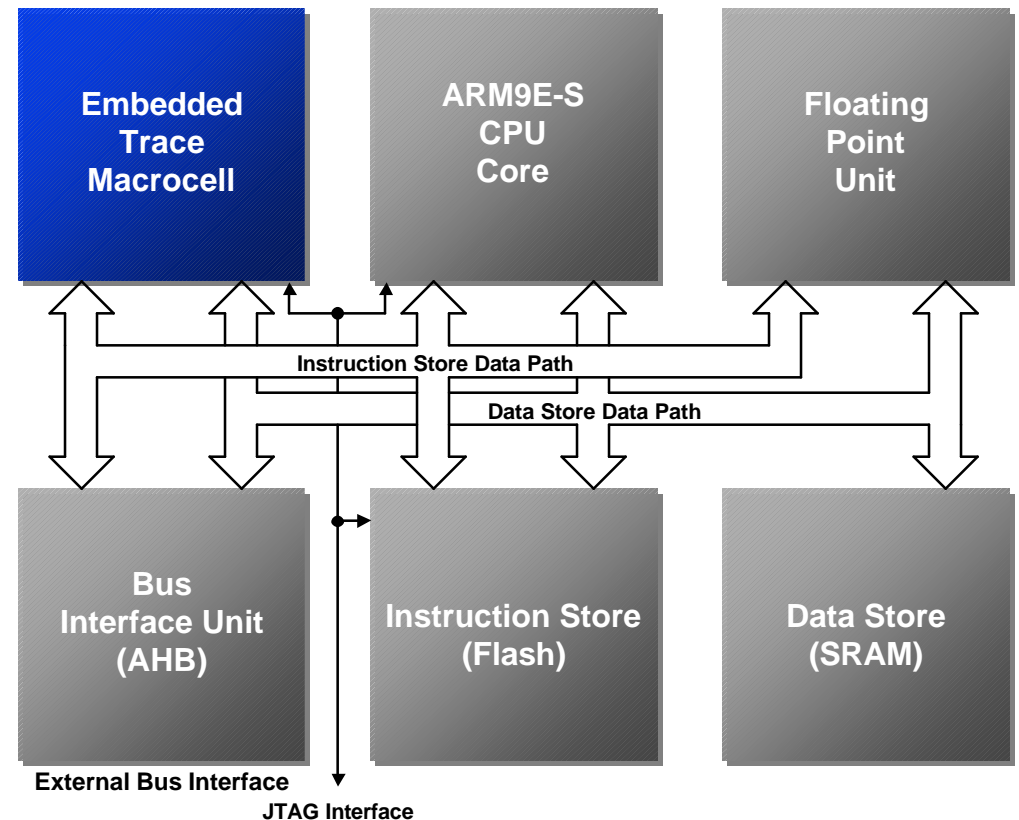
ARM9 Vectored Floating Point Unit

- IEEE 754 compliant
- Single- and Double-Precision Operations
- Register file: 32 SP/16 DP registers, Banked & Recirculating Modes Support Vector Operations
- High-Performance Vector Operations Overlap Load/Store Operations for Superscalar Performance
- 200 FIR filter MFlops @ 100 MHz
- Vector-Scalar & Vector-Vector Operations



ARM9 Embedded Trace Macrocell

- Monitors ARM Core Buses
- Passes Compressed Information Via JTAG to Trace Port Analyzer
- Debug Tools Retrieve Data From Analyzer and Reconstructs Historical View of Processor's Activity Including Data
- User-Definable Filters Allow Limitation of Information Captured In Search of Bug



System On Chip Peripherals

- **Application Specific Peripherals**

- RTEC, Real Time Engine Controller
- WSAJ, Wheel Speed/Acceleration/Jerk

- **Communication Peripherals**

- J1850VB, J1850 Protocol Controller / VPW / Byte Level Interface
- J1850VM, J1850 Protocol Controller / VPW / Message Level Interface
- SCI, Serial Communication Interface
- QSCI, Queued Serial Communication Interface
- SPI, Serial Peripheral Interface
- BSPI, Buffered Serial Peripheral Interface
- CAN, Control Area Network 2.0B

- **Microprocessor Specific Peripherals**

- NIROC, Non-Intrusive RAM Overlay Calibration
- 100MHz Memory (Flash) Bus Interface
- APIC, ARM Processor Interrupt Controller

- **General Purpose Peripherals**

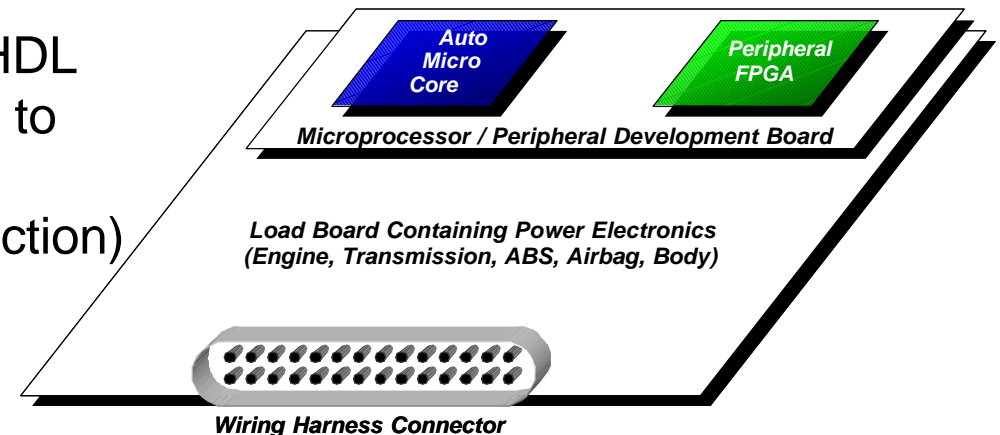
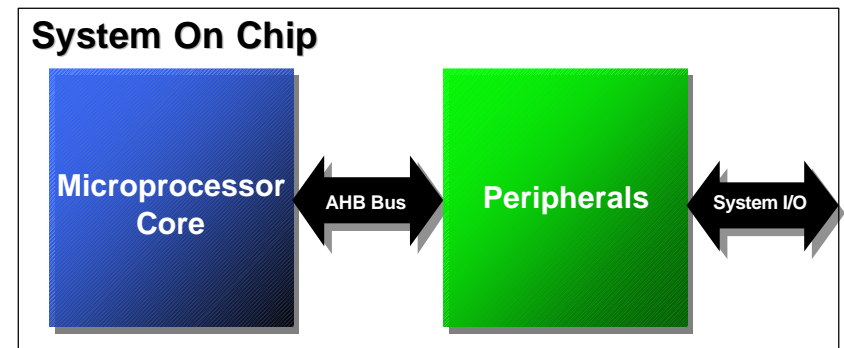
- GPIO, General Purpose Input Output
- EDGE, Edge Detect
- PACR, Pulse Accumulator
- ICAP, Input Capture
- OCOM, Output Compare
- PWM, Pulse Width Modulator

- **Customer Specific Peripherals**

System On Chip Development Platform

- **Micro / Peripheral Development Board**

- ✓ Includes Microprocessor Core - ARM9 Based (ARM7 and ARM10 Planned)
- ✓ Includes Integrated Memory (Code-1.25M Bytes Flash and Data-64K Bytes SRAM)
- ✓ Includes Advanced High Performance Bus Interface (AHB)
- ✓ Includes FPGA for Peripheral Implementation
- ✓ AIEC Peripherals Designed Using HDL Which Allows Targeting Peripherals to Virtually any Technology (FPGA for Prototyping, Standard Cell for Production)
- ✓ A-to-D, Digital Level Shifting



- **Load Board**

- ✓ Customer Specific Power Electronics

System On Chip Development Platform

- System Hardware and Software Run at Targeted Application Speed (>100MHz)
- Platform Supports In System Calibration (NIROC / ETM / JTAG Fully NEXUS Equivalent)
- Platform Supports Rapid Prototype Development (NIROC / ETM / JTAG)
- Platform Supports Co-Design (Hardware/Software)
- Prototype Entire System before Committing to Silicon
- Development Platform Compatible with Production Intent Silicon