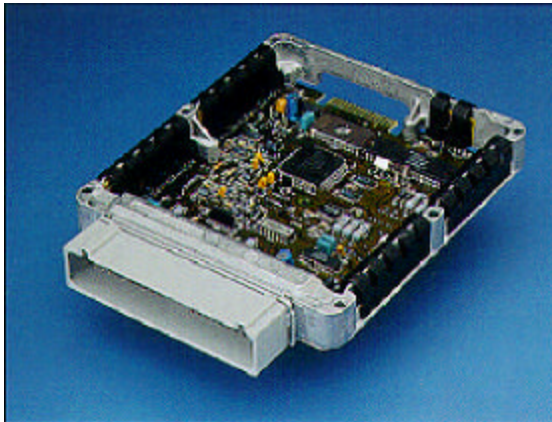




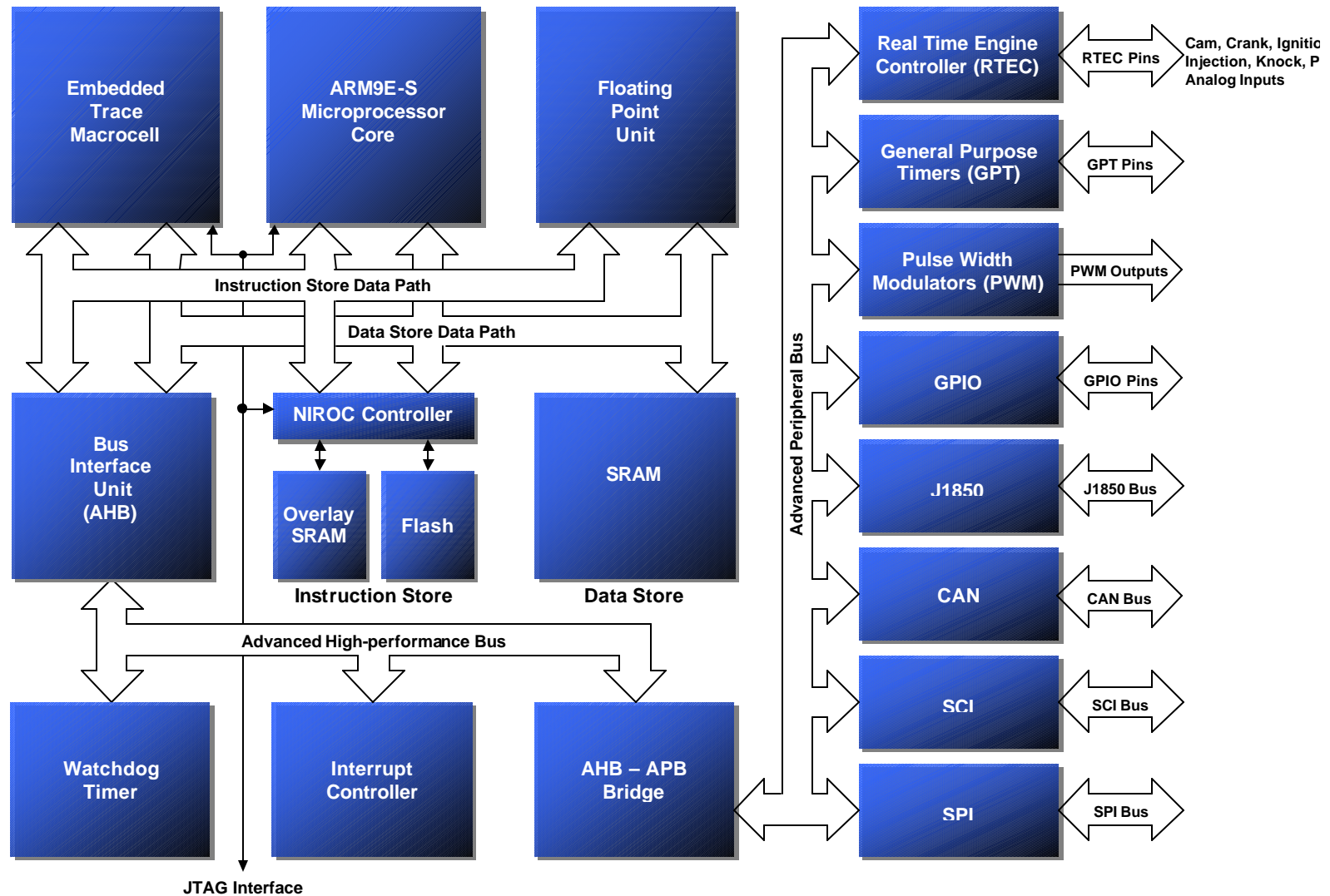
ARM9E-S Based Powertrain Controller System On Chip



Presentation Overview

- **ARM9E-S Based Powertrain Controller SoC Block Diagram**
- **Memory Architecture (Enhanced Tightly Coupled Flash)**
- **Non Intrusive RAM Overlay Calibration (NIROC)**
- **ARM Processor Interrupt Controller (APIC)**
- **Real Time Engine Controller (RTEC)**
- **Communication Peripherals (SCI, SPI, CAN, J1850)**
- **Business Model**

ARM9E-S Based Powertrain Controller SoC Block Diagram



Memory Architecture

Memory Architecture Alternatives

- **Memory Caching Systems Not Considered Because of High Cost and Unpredictable Latencies (Generally in Real Time Control System Like Powertrain Latencies Must be Known)**
- **Instruction Store In Flash Connected Via Advanced High-performance Bus (AHB) Interface with No Tightly Coupled Static RAM Instruction Store “*External Flash*”**
- **Instruction Store In Flash Connected Via AHB Interface with Tightly Coupled Static RAM Instruction Store (Time Critical Routines Moved to Tightly Coupled SRAM at Boot) “*Pseudo Cache*”**
- **Instruction Store Tightly Coupled Flash Executing at Maximum Access Time (20ns) CPU Running at 50MHz “*Tightly Coupled Flash*”**
- **Instruction Store Tightly Coupled Flash Executing at 2X Maximum Flash Access Time (20ns) CPU Running at 100MHz “*Enhanced Tightly Coupled Flash*”**

Memory Architecture Alternative

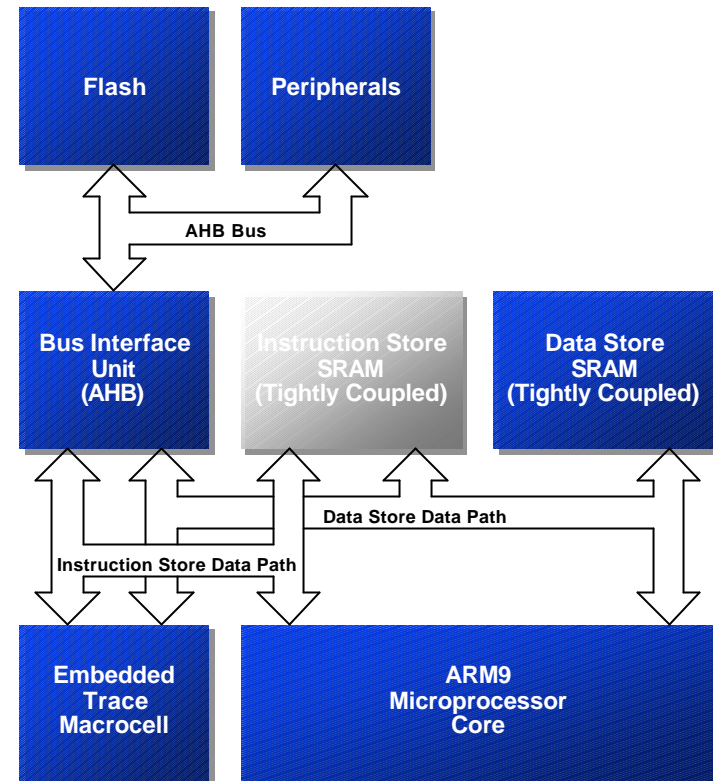
“External Flash”

- ***External Flash Advantages***

- Lowest Cost (No Duplication of Memory for Instruction Store)
- Ease of Programming (All Routines Execute at Same Speed, No Memory Partitioning)

- ***External Flash Disadvantages***

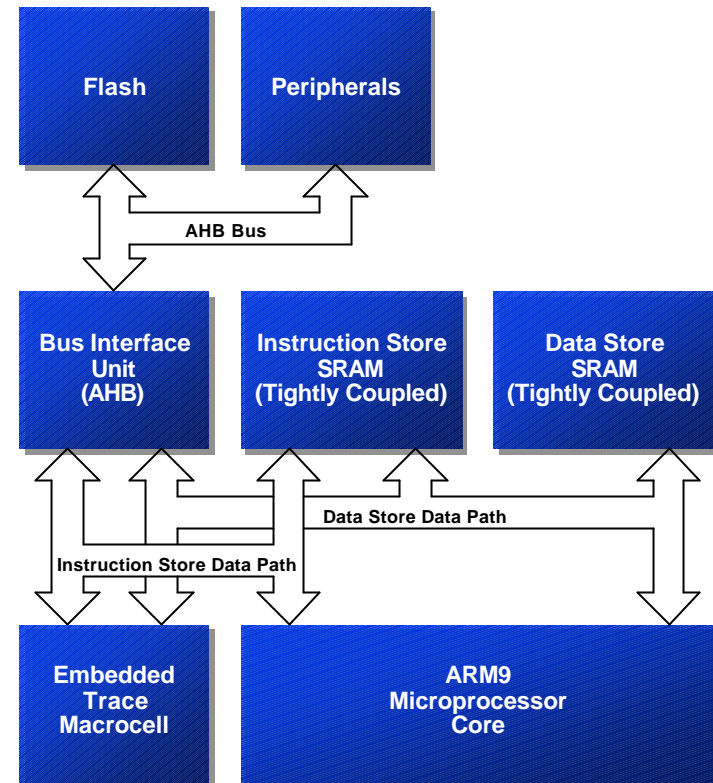
- Lowest Performance (Stall Instruction Fetch On Data Access from Peripherals, Von Neumann Architecture)



Memory Architecture Alternative

“Pseudo Cache”

- **Pseudo Cache Advantages**
 - Higher Performance than “External Flash” (Time Critical Routines Moved to Tightly Coupled SRAM, Harvard Architecture)
- **Pseudo Cache Disadvantages**
 - Highest Cost (Duplicated Memory – Instruction Store Flash and SRAM)
 - Lower Performance than “Tightly Coupled Flash” and “Enhanced Tightly Coupled Flash” (Instruction Stall Potential When Peripheral Accessed)
 - Memory Partition Issues (Time Critical Routines Stored in Tightly Coupled SRAM, How Much RAM is Enough?, etc.)



Memory Architecture Alternative

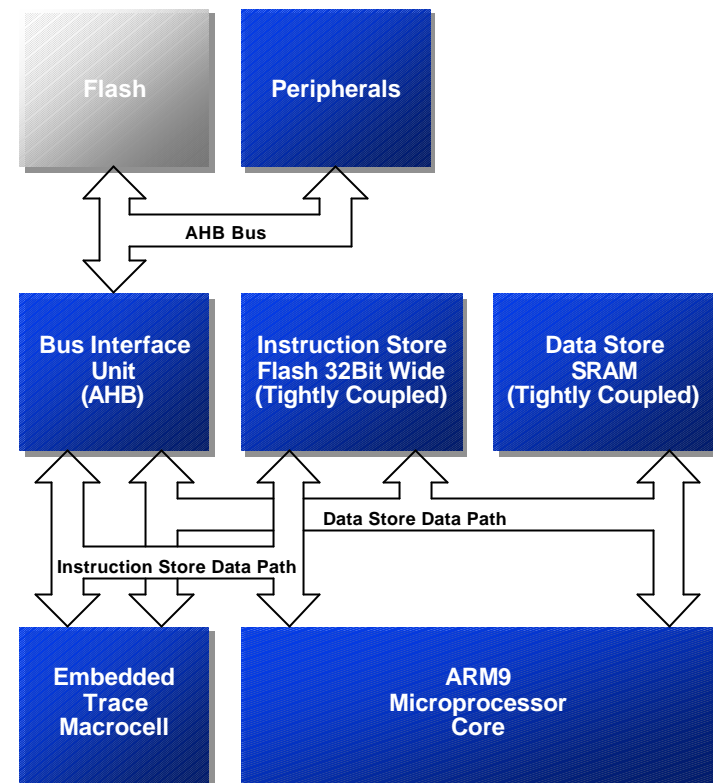
“Tightly Coupled Flash”

- **Tightly Coupled Flash Advantages**

- Higher Performance than “Pseudo Cache” (All Routines in Tightly Coupled Flash, Harvard Architecture)
- Ease of Programming (All Routines Execute at Same Speed, No Memory Partitioning)
- Lowest Cost (No Duplication of Memory for Instruction Store)

- **Tightly Coupled Flash Disadvantages**

- Lower Performance than “Enhanced Tightly Coupled Flash” (Limited by Flash Access Time 20ns, Processor Limited to 50MHz)



Memory Architecture Alternative

“Enhanced Tightly Coupled Flash”

- *Enhanced Tightly Coupled Flash*

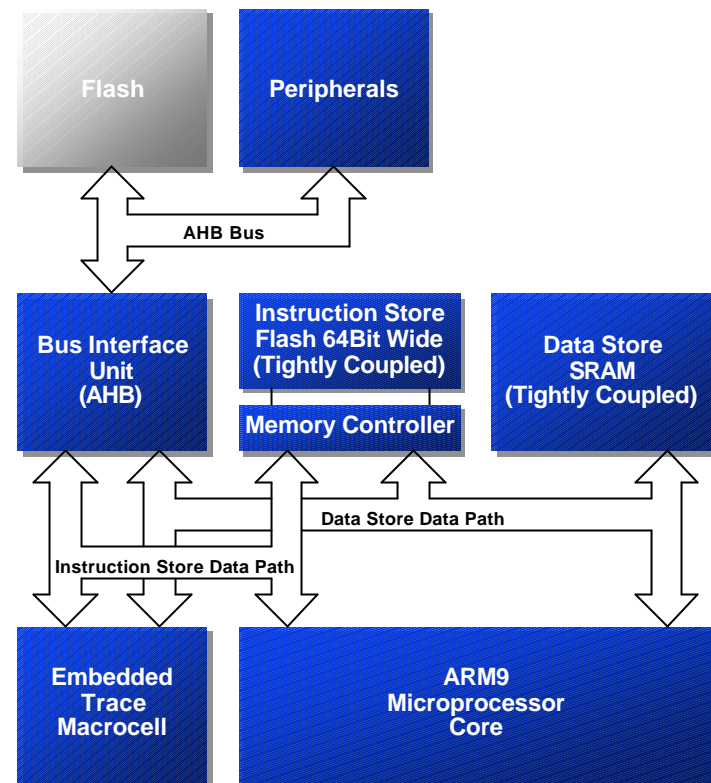
Advantages

- Highest Performance (Wider Data Path Fetches 2 Instructions, Processor Runs at 100MHZ)
- Ease of Programming (All Routines Execute at Same Speed, No Memory Partitioning)
- Lowest Cost (No Duplication of Memory for Instruction Store)
- Expandability to > 64 Bits

- *Enhanced Tightly Coupled Flash*

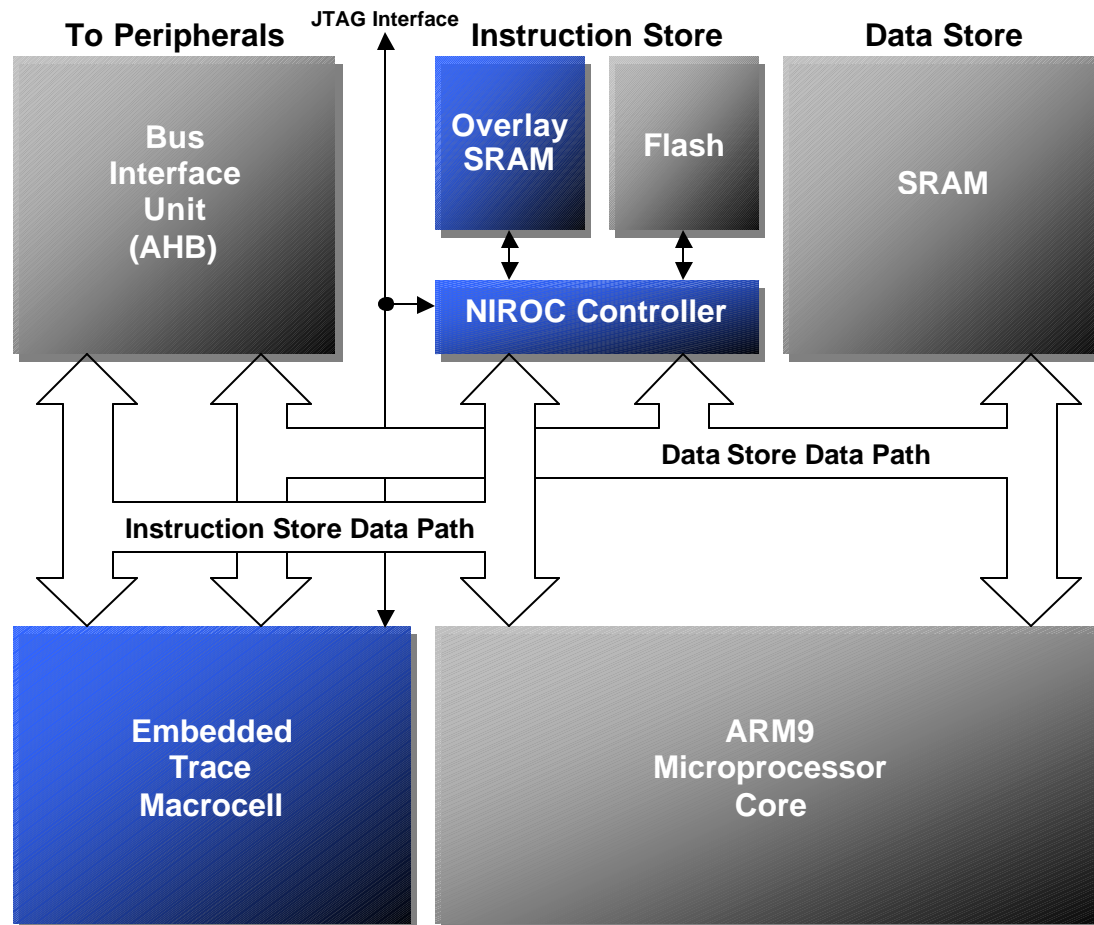
Disadvantages

- Single Clock Stall On Branch



Non Intrusive RAM Overlay Calibration

Non-Intrusive RAM Overlay Calibration (NIROC) Block Diagram



Non-Intrusive RAM Overlay Calibration Strategy

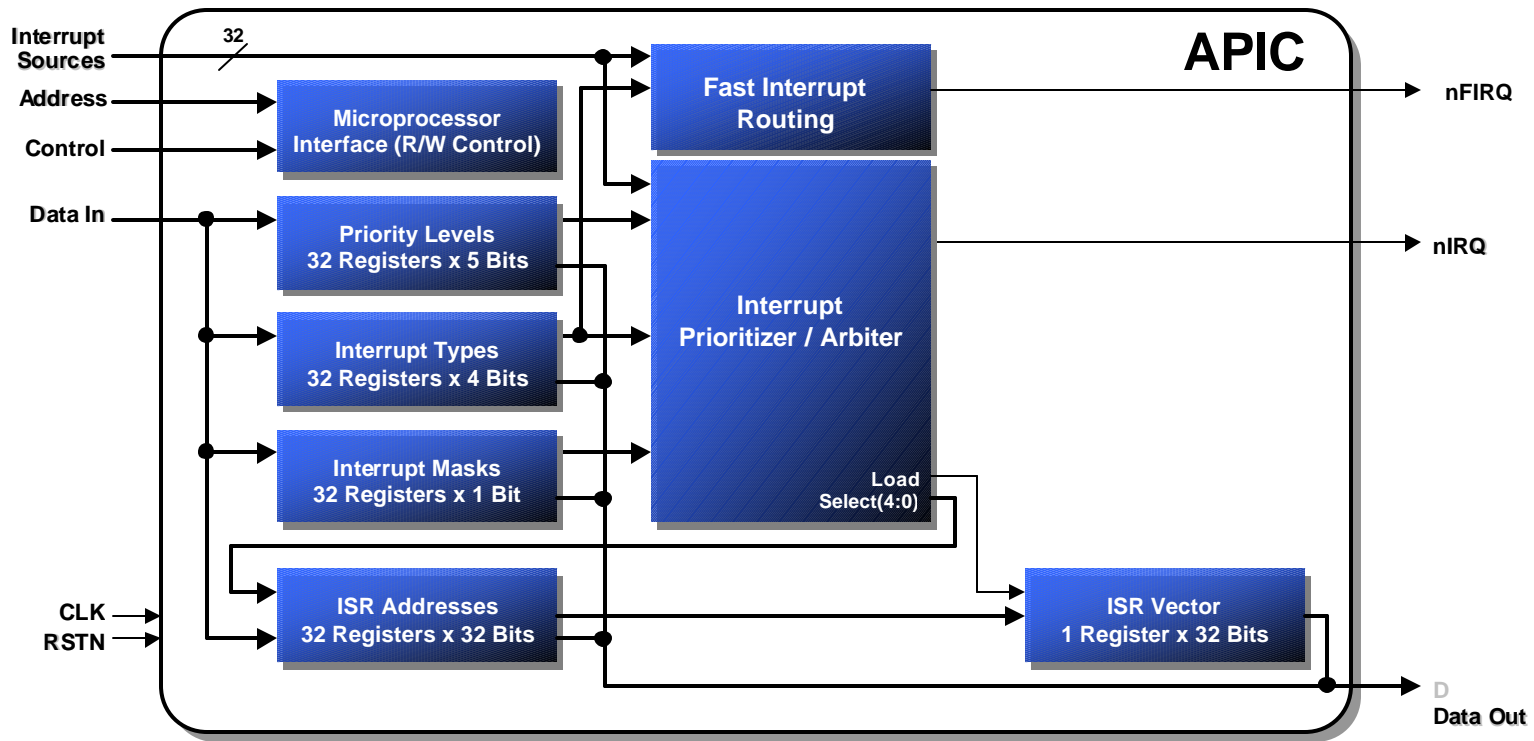
- **Monitor Feedback Variables**
 - Embedded Trace Macrocell Automatically Monitors Control and Result Variables (Completely Non-Intrusive)
- **Copy Calibration Data to RAM Overlay**
 - Multi-ICE Tool Downloads Calibration Data through JTAG Port to NIROC Controller
 - NIROC Controller Loads RAM Overlay Independent of Microprocessor Flash Accesses (Completely Non-Intrusive)
- **RAM Overlay Enabled**
 - Multi-ICE Tool Downloads Command through JTAG Port to Enable RAM Overlay for Instantaneous Bank Switching of Coherent Data
 - NIROC Intercepts Microprocessor Calibration Data Accesses from Flash and Stuffs RAM Overlay Data to Microprocessor Bus
- **Instruction Store Re-Flashed with New Calibration Data**
 - Existing Flashing Routines Used to Re-Flash Instruction Store

Non-Intrusive RAM Overlay Specification

- **RAM Overlay for Modification of Calibration Data**
 - Writeable Via JTAG Interface (Non-Intrusive)
 - Writeable Via Microprocessor Core (Support Legacy Serial Port Calibration)
 - 2K x 32bits (8K Bytes)
 - 16 RAM Overlay Segments at 128 x 32bits (512 Bytes Each)
 - Instantaneous Bank Switching of Overlay Segments – Can Be Controlled by Application Software to Be Position Synchronous
- **Embedded Trace Macrocell for Monitoring of Feedback Variables**
 - Monitor of 16 Individual Variables or 8 Address Ranges of Variables or Any Combination Thereof
 - Application Software Controls Trace Updates of Variables Which Can Be Asynchronous, Time Synchronous, Or Position Synchronous
- **Rapid Prototype Development**
 - ASCET Support

ARM Processor Interrupt Controller

ARM Processor Interrupt Controller Block Diagram



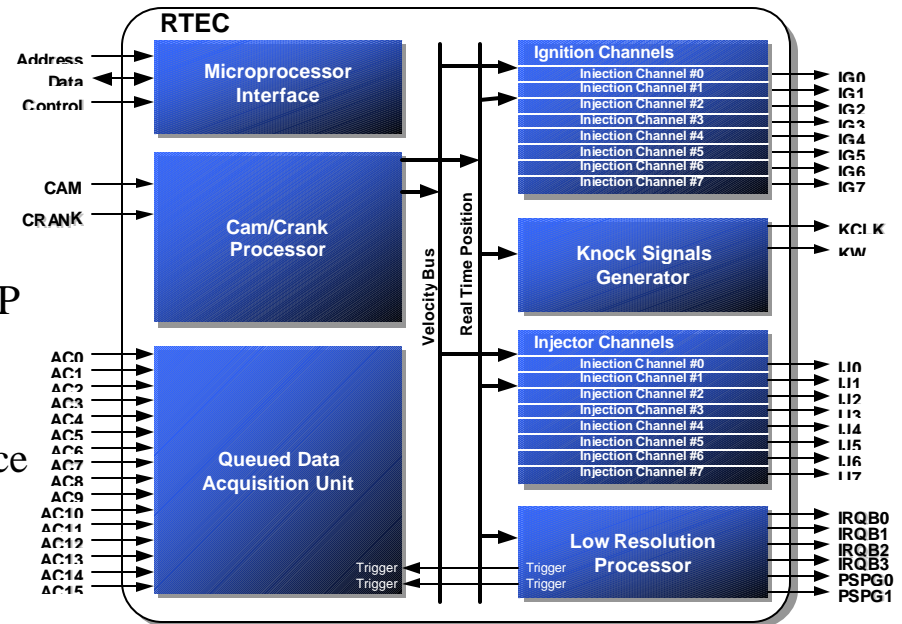
ARM Processor Interrupt Controller Features

- Compatible with ARM7TDMI and ARM9TDMI microprocessor cores
- Supports thirty-two interrupt sources for the nIRQ interrupt
- Any interrupt source can be routed to the nFIRQ interrupt
- Hardware interrupt vectoring reduces interrupt service routine latency
- Full hardware prioritization of interrupt sources
- Interrupts of lower priority levels automatically masked while interrupt is serviced
- Round-robin arbitration for interrupts at the same priority level ensures starvation-free operation under the heaviest of loading conditions
- Interrupt sources programmable with unique interrupt service routine addresses
- Thirty-two priority levels, programmable for each interrupt source
- Interrupts can have either a software or hardware source, Hardware interrupts can be active high or low, and edge or level-sensitive
- Masking programmable on a per-interrupt source basis

Real Time Engine Controller (RTEC)

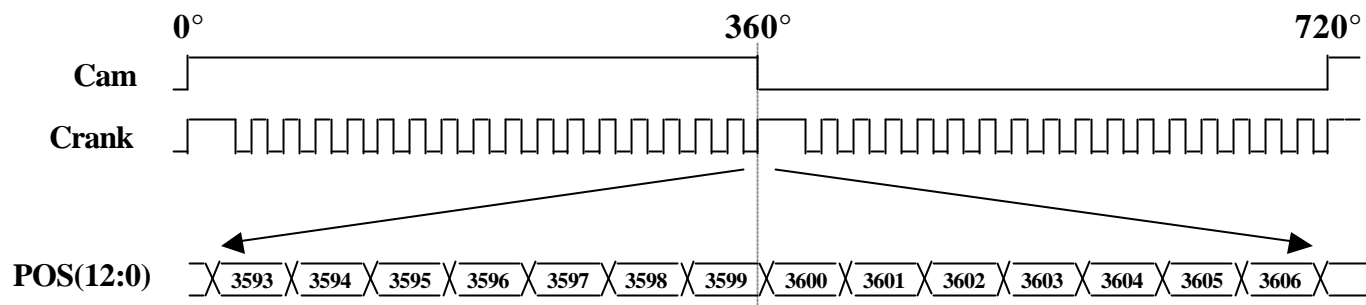
Real Time Engine Controller (RTEC) Block Diagram

- **Cam / Crank Processor**
 - Accepts Arbitrary Tooth Patterns
 - Extremely Fast Lock Time
 - Cam Only Limp Home
 - Runs Completely Independent of uP
- **Ignition Channels / Knock Signals**
 - Wired OR Outputs Support Virtually all Ignition Strategies
 - Two uP Writes Control Ignition Sequence
 - Knock Signal Generation Independent of uP
- **Injection Channels**
 - Flexible 3 Pulse/Cycle Generation
 - Single uP Write Controls Injection Sequence
- **Low Resolution Processor**
 - Automatic Triggering of A-to-D
 - Precision Timing (Misfire Detection)
- **Queued Data Acquisition Unit**
 - 5 Independent Triggers (2 Position, 2 Time Based, 1 Software)
 - Queue Depth User Selectable

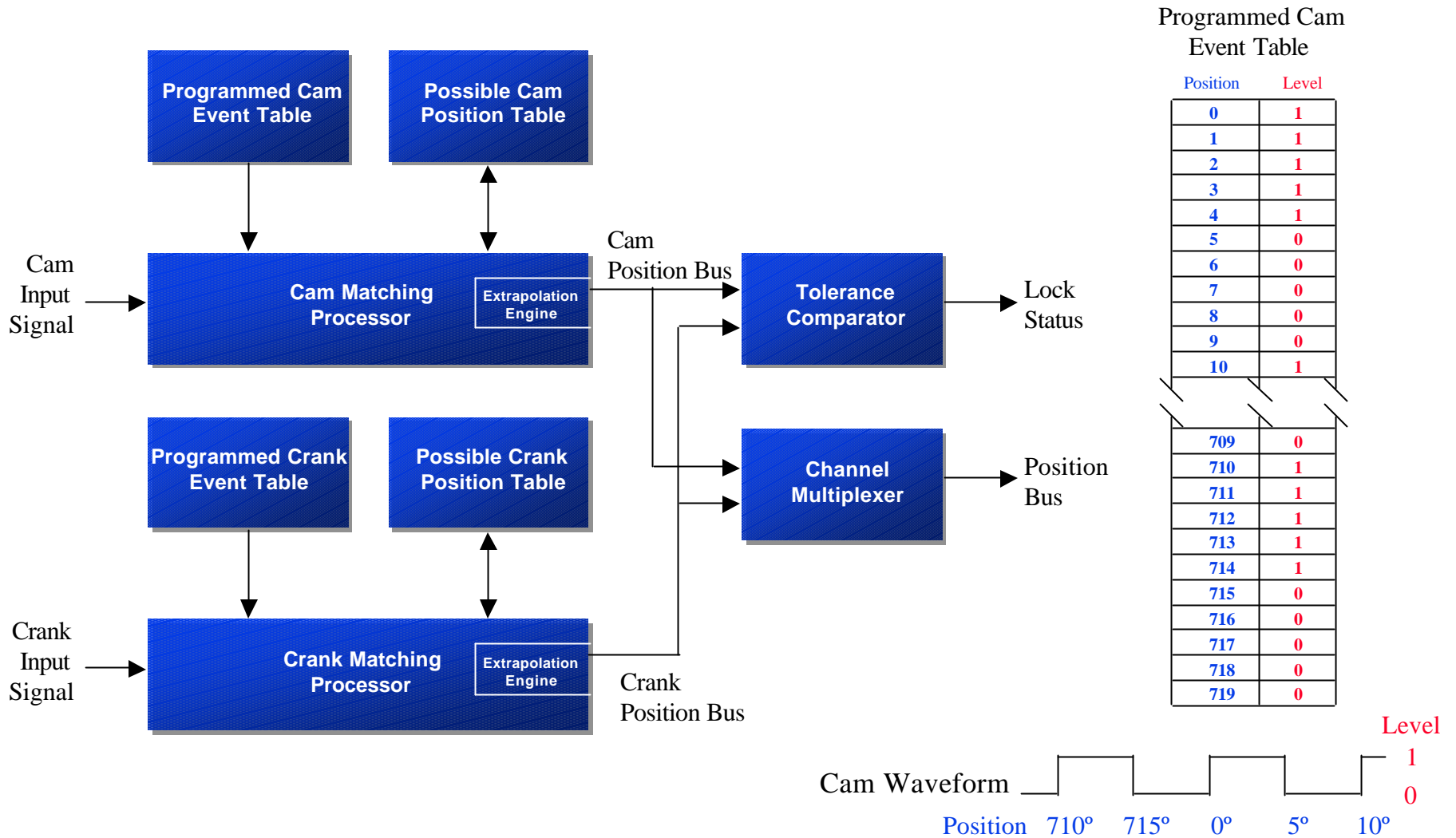


Cam / Crank Processor Module (CCPM) Functionality

- **Angular Position Tracking**
 - Angular Position Tracked Without Microprocessor Intervention
 - Real Time Position Bus (Range = 0.0°-719.9°, Resolution = 0.1°)
- **Independent Cam and Crank Channels**
 - Position Extrapolation On Cam Only or Crank Only Input Signals
- **Arbitrary Cam and Crank Waveforms**
 - Simple Configuration Through Table Programming



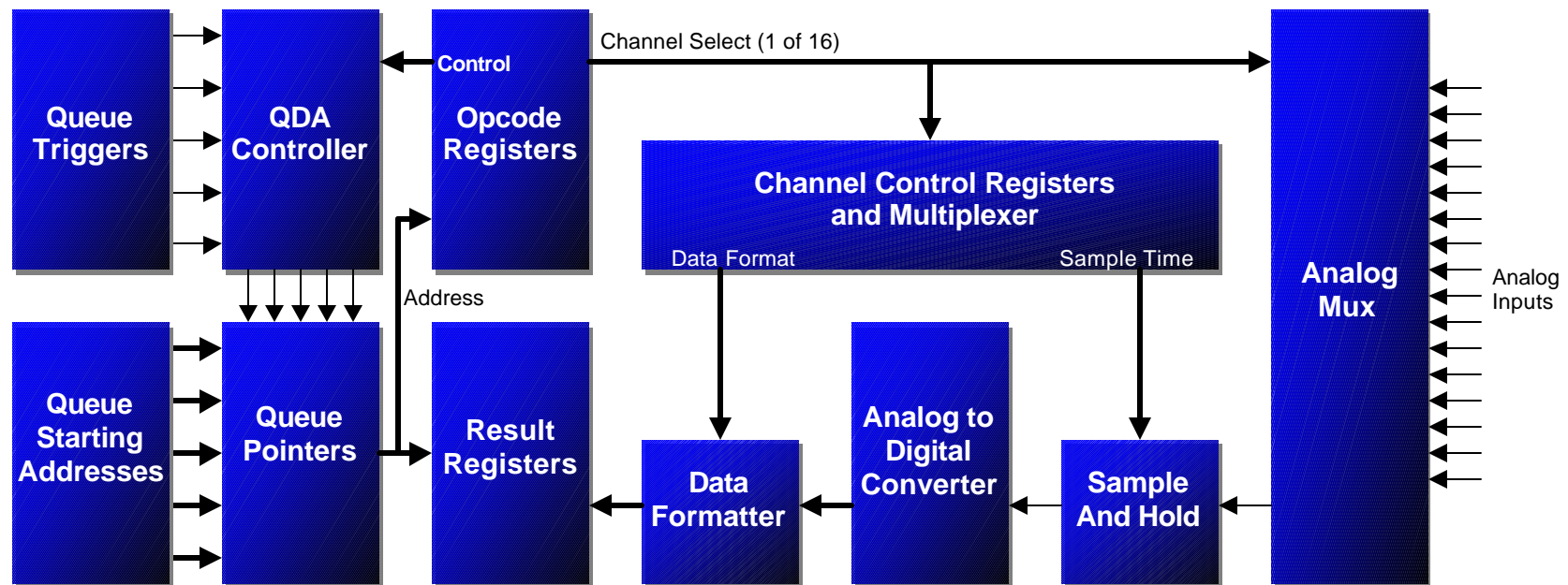
Cam / Crank Processor Module (CCPM) Block Diagram



RTEC Data Acquisition Module (DAQM) Functionality

- **Automatically Acquires Analog Signals**
 - Once Initialized, Requires No Further Microprocessor Intervention for Signal Acquisition
- **Analog to Digital Conversion - Position, Time and Software Triggered**
 - 2 Independent Position Queues from 1 to 64 Acquisitions
 - 2 Independent Time Based Queues with Programmable Intervals
 - 1 Software Triggered Queue for On Demand Data Acquisition
- **Analog to Digital Converter Specifications (-40° to 125°, ±10% Supply)**
 - 16 Channels, 10-Bit Resolution, ±1/2 LSB Accuracy
 - 5uS Conversion Time, Guaranteed Monotonicity and No Missing Codes

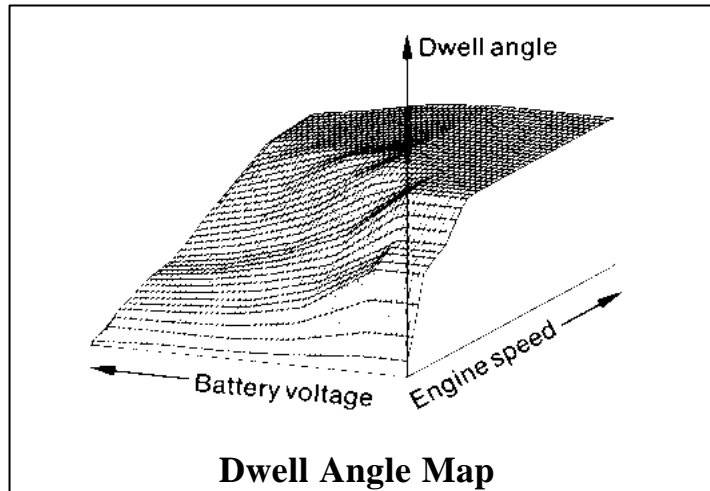
RTEC Data Acquisition Module (DAQM) Block Diagram



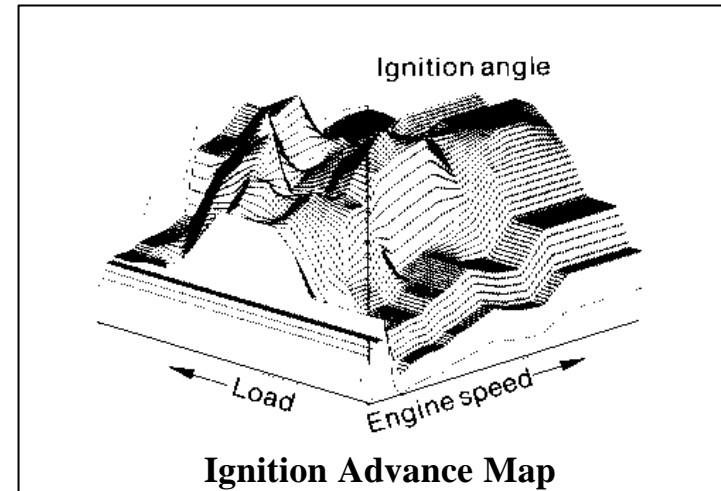
RTEC Ignition Channel Module (IGCM) Functionality

- **Precision Ignition Timing**
 - 30uS Resolution Dwell Time Over Entire Operating Range (>500RPM)
 - 0.1° Resolution Ignition Advance Angle
- **Simplified Programming**
 - Single Write to Program Dwell Time
 - Single Write to Program Ignition Advance Angle
 - Ignition Channel Continues Without uP Intervention
 - Dwell Time and Advance Angles Programmed Synchronous or Asynchronous to Engine Events
- **Increased Performance**
 - Real Time Ignition Timing Per Spark for Increased Fuel Economy and Reduced Emissions

Ignition Programming (Dwell and Ignition Advance Angles)



Robert Bosch GmbH, Automotive Electric/Electronic Systems



Robert Bosch GmbH, Automotive Electric/Electronic Systems

Dwell Angle Programming

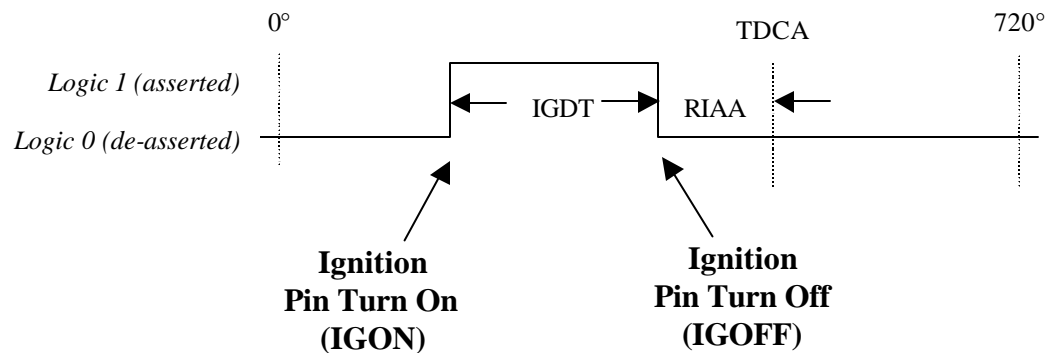
- 1) Read Battery Voltage from DAQM
- 2) Read Engine Velocity from CCPM
- 3) Fetch Dwell Angle from Map
- 4) Write Relative Dwell Angle to IGCM

Ignition Advance Programming

- 1) Read Manifold Pressure from DAQM
- 2) Read Engine Velocity from CCPM
- 3) Fetch Ignition Advance from Map
- 4) Write Ignition Advance Angle to IGCM

- **Total of 8 Operations for Ignition Programming of a Cylinder**

RTEC Ignition Channel Output Waveform



$$\text{IGOFF} = \text{TDCA} - \text{RIAA}$$

$$\text{IGON} = \text{IGOFF} - (\text{IGDT} * \text{Velocity})$$

TDCA - Top Dead Centers for Each Ignition Channel are Programmed Immediately after RESET

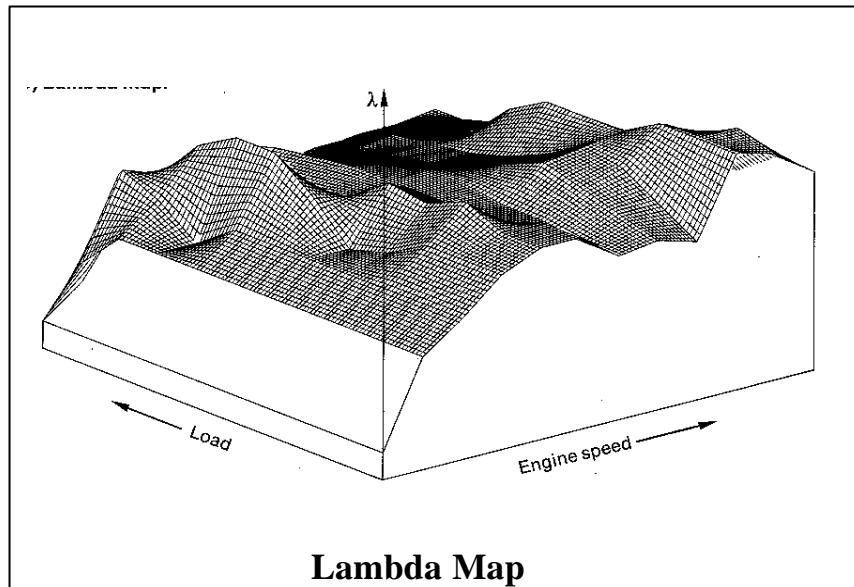
RIAA - Relative Ignition Advance Angle Programming Changes Take Effect Immediately

IGDT - Ignition Dwell Times Programming Changes Take Effect Immediately

RTEC Injector Channel Module (IJCM) Functionality

- **Precision Fuel Metering**
 - 4uS Resolution Injector On Time Over Entire Operating Range (>500RPM)
 - 0.1° Resolution Injector On/Off Angle
- **Simplified Programming**
 - Single Write Instruction for Programming Total Commanded Pulse Width
 - Injector Channel Continues Without uP Intervention
 - Total Commanded Pulse Width Programmed Synchronous or Asynchronous to Engine Events
- **Increased Performance**
 - Real Time Injector Timing Per Combustion for Increased Fuel Economy and Reduced Emissions

Injector Programming (On Angle and Duration)

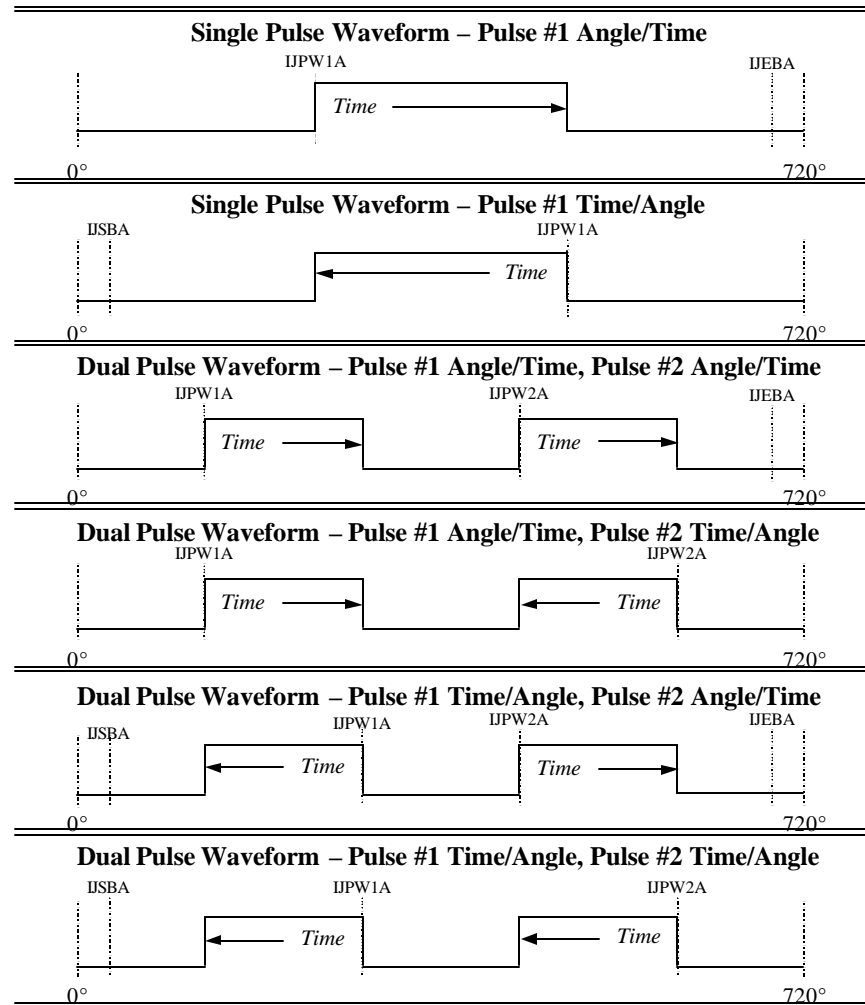


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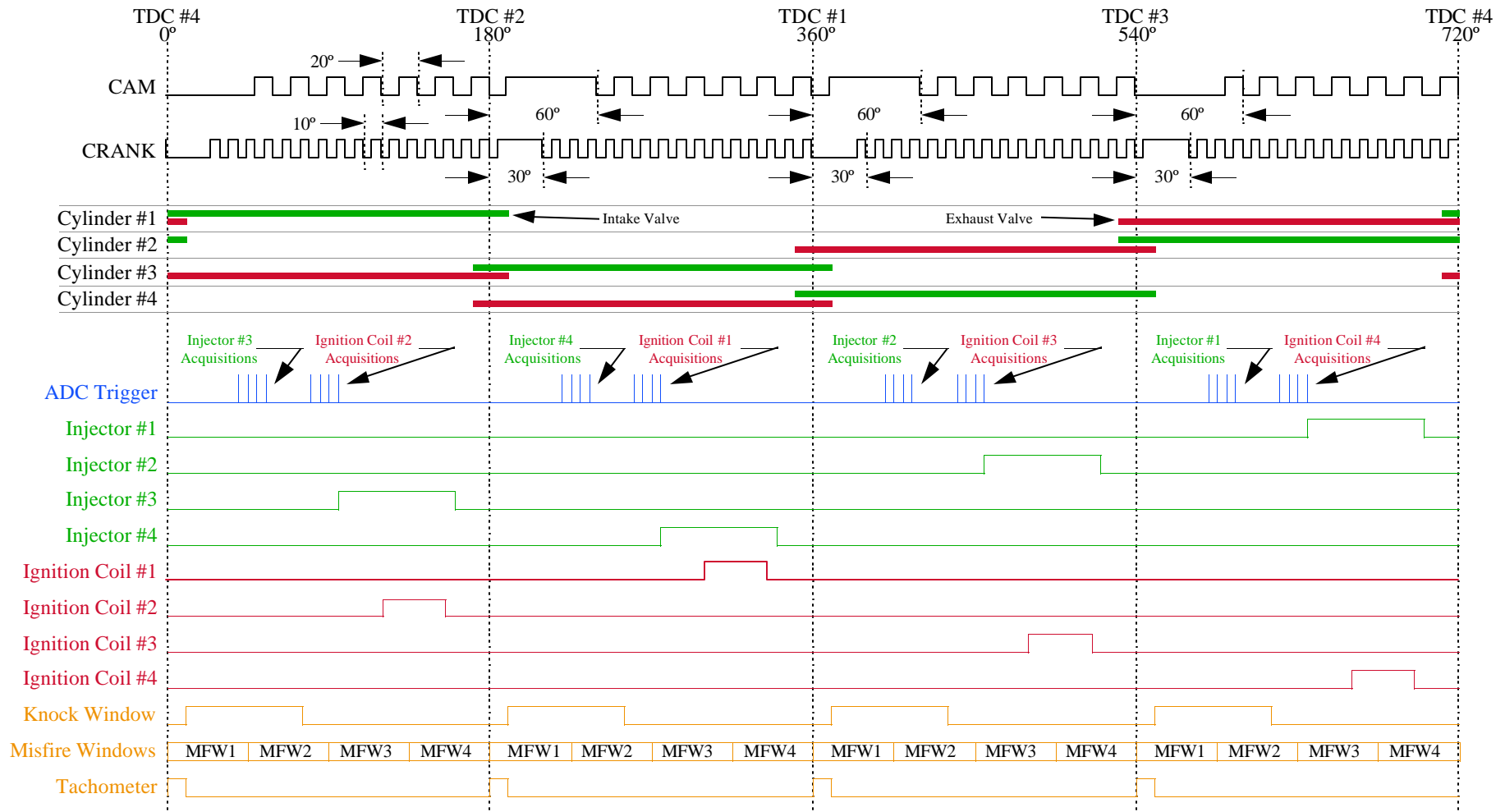
Injector Programming

- 1) Read Manifold Absolute Pressure from DAQM
- 2) Read Engine Velocity From CCPM
- 3) Fetch Air/Fuel Ratio (Lambda) from Map
- 4) Read Mass Air Flow from DAQM
- 5) Read Battery Voltage from DAQM
- 6) Read Engine Temperature from DAQM
- 7) Read Air Temperature From DAQM
- 8) Read O₂ Sensor from DAQM
- 9) Read Throttle Valve Angle from DAQM
- 10) Read Throttle Valve Position from GPIO
- 11) Calculate Injector Period
- 12) Write Injector Total Commanded Pulse Width

RTEC Injector Channel Module (IJCM) Output Waveform



Real Time Engine Controller Timing Diagram

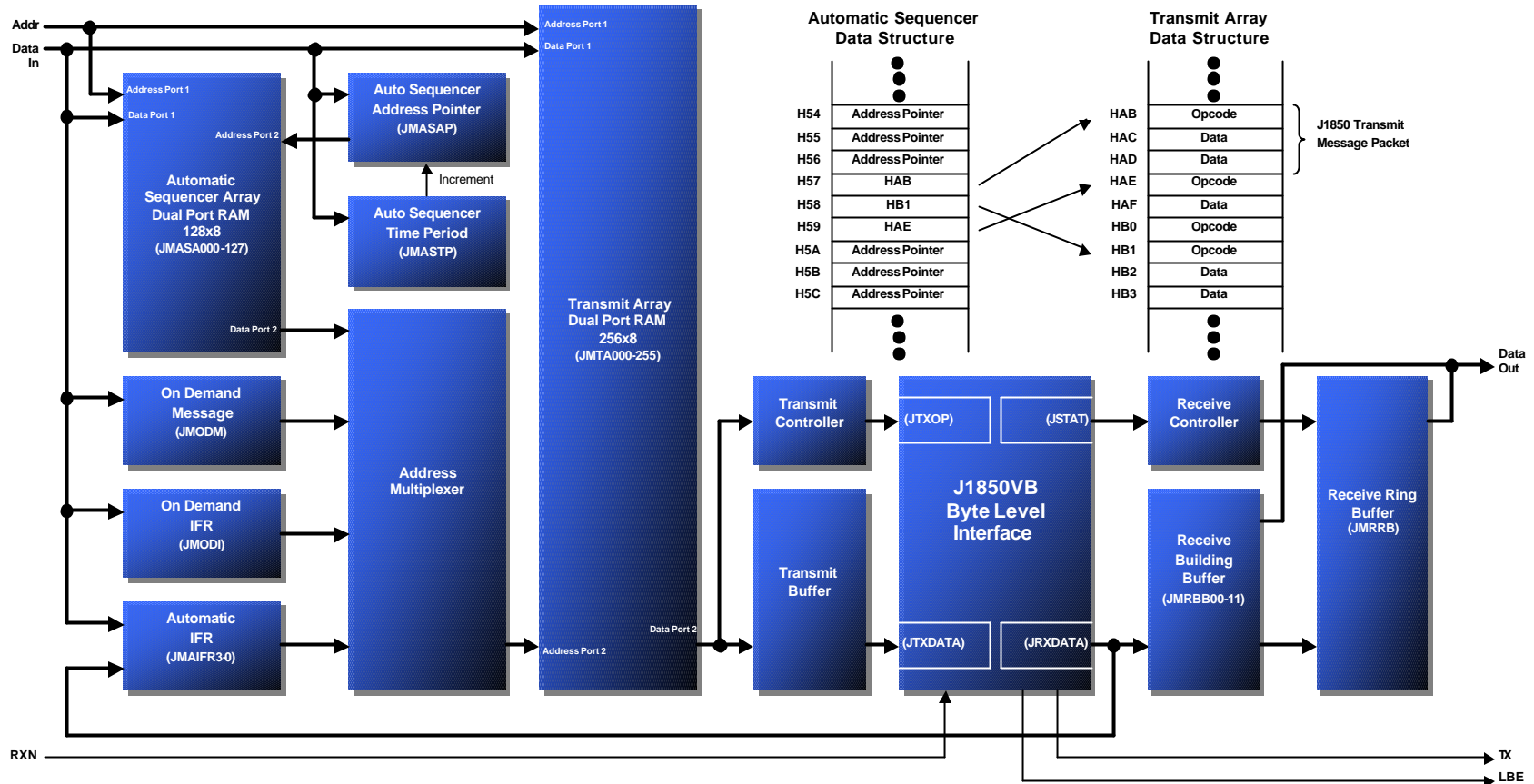


Communication Peripherals

Communication Peripherals

- **Serial Communication Interface (SCI)**
- **Queued Serial Communication Interface (QSCI)**
- **Serial Peripheral Interface (SPI)**
- **Control Area Network (CAN)**
- **Variable Pulse Width Modulated Byte Level J1850**
- **Variable Pulse Width Modulated Message Level J1850**

Message Level J1850 Block Diagram



- **Interrupt Free Transmission (No Microprocessor Intervention Required)**
- **Reduced Interrupt Reception (Message Filtering)**
- **Automatic In Frame Response (No Microprocessor Intervention Required)**

Business Model

Business Model

- **AIEC's Primary Focus is the Development of Custom System On Chip (SoC) for Automotive Industry**
- **Custom SoC Allows Customer to Differentiate Product As Opposed to Standard Product**
- **Significant Advantage of AIEC's Business Model Provides the Customer with a Design That is Independent of Semiconductor Supplier**
- **Design Effectively Becomes a Commodity and Can Be Sourced by Semiconductor Supplier of Choice**
- **Significant Cost Savings and Higher Levels of Service are Achieved Through Commodity Sourcing**