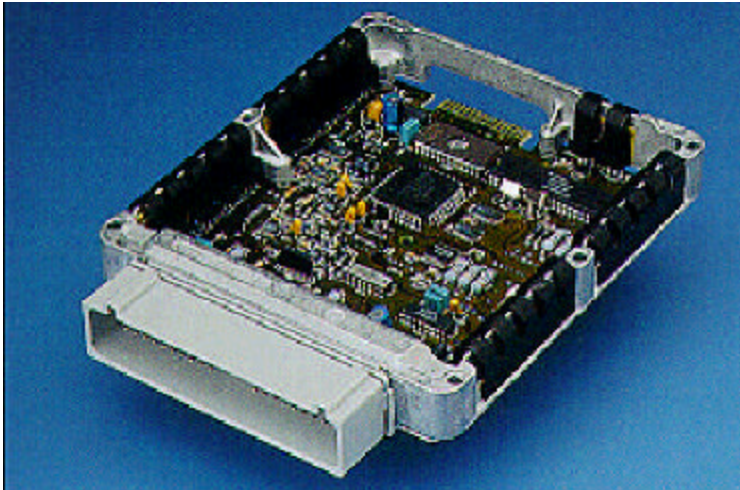


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# ARM Automotive Conference



## AIEC Automotive System On Chip (SoC) Development Platform



**Novi, Michigan  
June 6, 2001**

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# Presentation Overview

- **Automotive Integrated Electronics Corporation**
  - ✓ **Company Background**
- **Automotive System On Chip Block Diagram**
  - ✓ **Microprocessor/Memory/Application Specific Peripherals**
- **Automotive System On Chip Microprocessor Core**
  - ✓ **ARM Microprocessor Cores**
- **Automotive System On Chip Memory Architecture**
  - ✓ **Non Intrusive RAM Overlay Calibration (NIROC)**
- **Automotive Microcontroller Peripherals**
  - ✓ **Real Time Engine Controller (RTEC)**
- **Automotive System On Chip Development Environment**
  - ✓ **Development Environment and Hardware**

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# Automotive Integrated Electronics Corporation

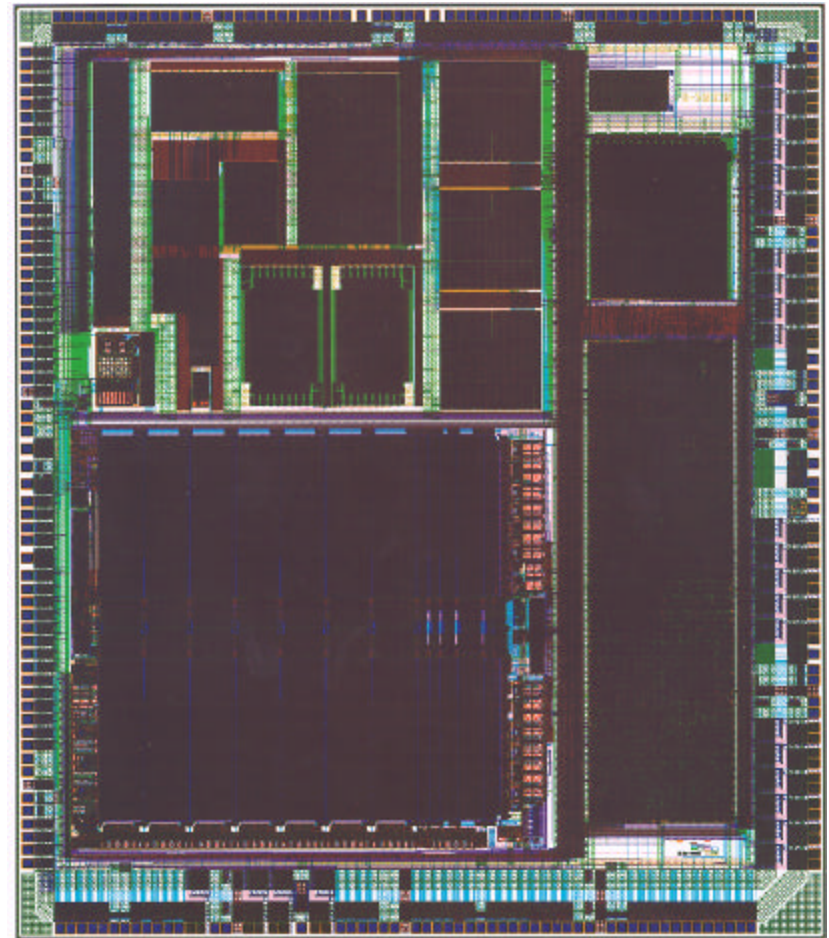
**Established in 1992 to Design Application Specific Integrated Circuits (ASICs) for the Automotive Industry**

**Designed 5 Generations of Engine Control ASICs and 4 Generations of Transmission Control ASICs for Major Automotive OEM**

**Comprehensive Quality Plan Using QS-9000 Advance Product Quality Planning (APQP), Design Failure Mode and Effects Analysis (DFMEA), 99% Fault Grading, IDDQ Testing**

**Primary Goal - Differentiate Customer's Products over Competition with Increased Performance at Reduced Cost**

**Clear Understanding That Our Success Depends on Our Customer's Success**



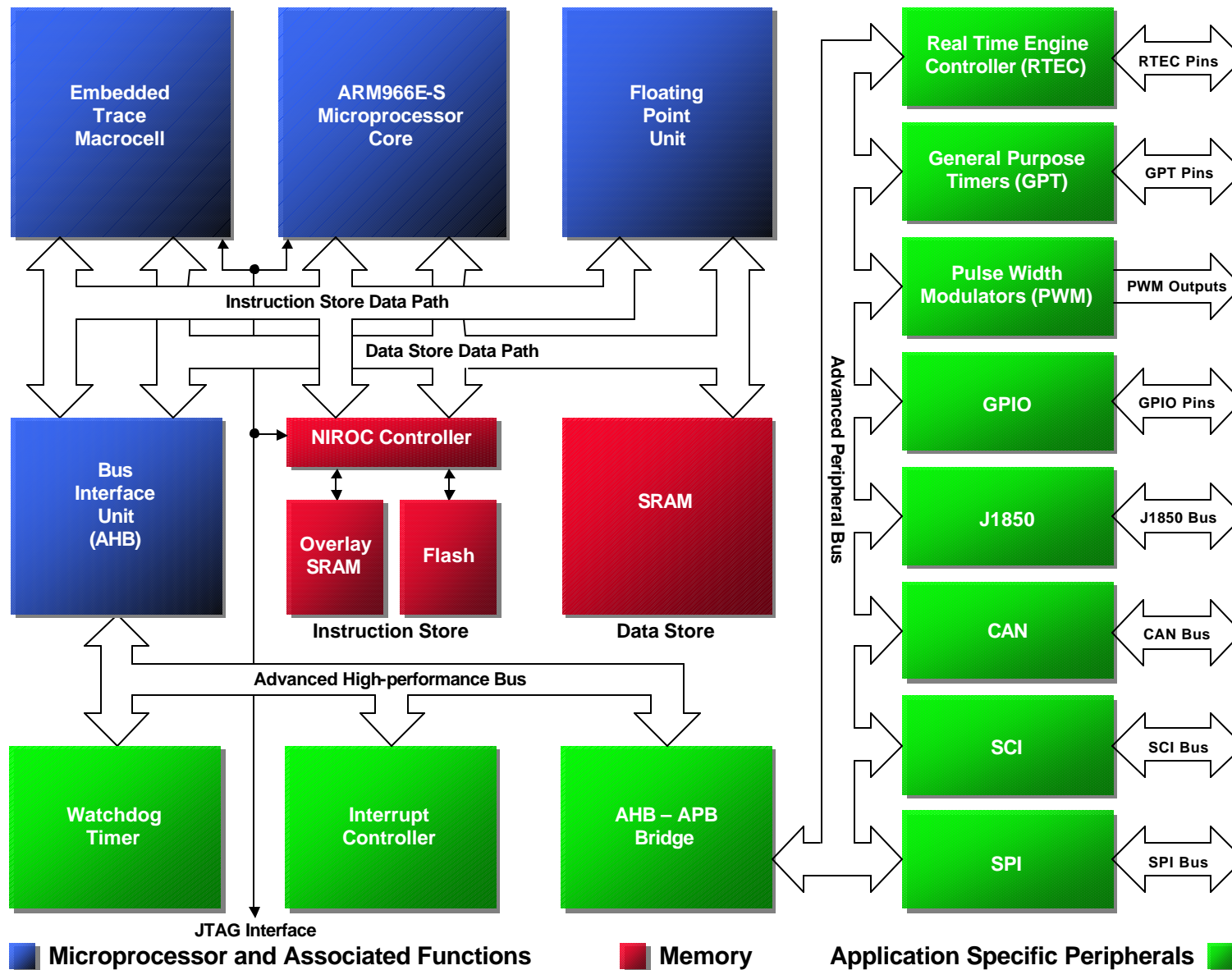
**System On Chip Transmission Controller  
(CPU, Flash, RAM, Application Specific Peripheral)**

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# Automotive System On Chip Block Diagram

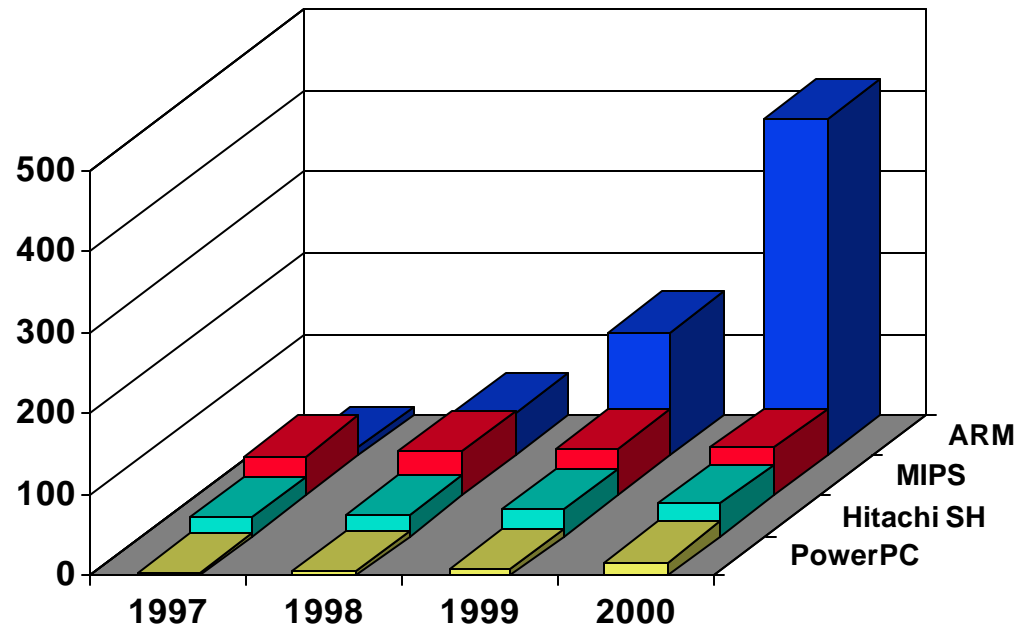


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# ARM Microprocessor Cores



## ARM Embedded Processor Market Share

- ARM Leads World Supply of Embedded 32-RISC Microprocessors
- ARM CPU for All Applications (Cost Sensitive / High Performance)
- Future Scalability through Object Code Compatible CPUs
- Comprehensive Development Tools
- Multiple Sourcing

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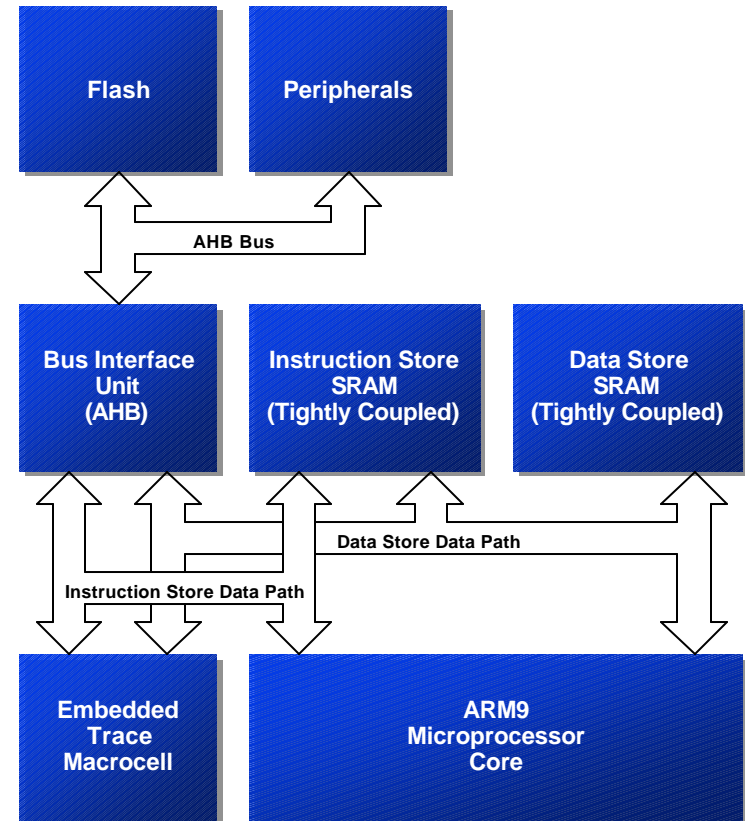
# Memory Architecture Alternative #1 “Cached System”

- **Cached System Advantages**

- Highest Performance for Instructions in Tightly Coupled Instruction Store SRAM (High Speed Instruction Store SRAM)

- **Cached System Disadvantages**

- Highest Cost (Duplicated Memory – Instruction Store Flash and SRAM)
- Large Latencies Associated with Caching (Difficult to Manage in Real Time Control Systems)



# Memory Architecture Alternative #2

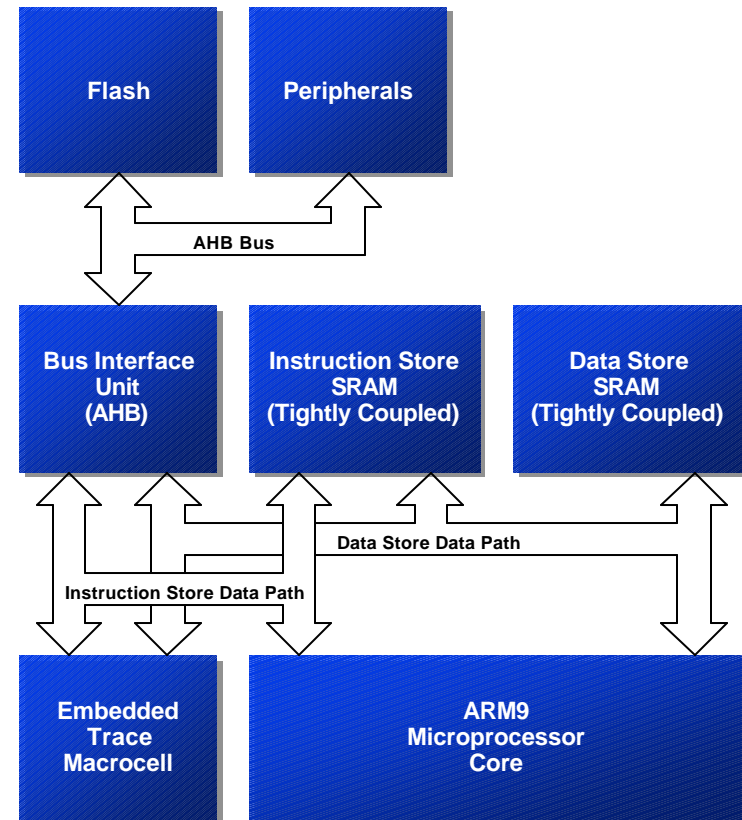
## “Pseudo Cache”

- **Pseudo Cache Advantages**

- Highest Performance for Locked Down Code (Time Critical Routines Moved to Tightly Coupled SRAM, Harvard Architecture)

- **Pseudo Cache Disadvantages**

- Highest Cost (Duplicated Memory – Instruction Store Flash and SRAM)
- Low Performance for Flash Based Code
- Memory Partition Issues (Time Critical Routines Stored in Tightly Coupled SRAM, How Much RAM is Enough?)



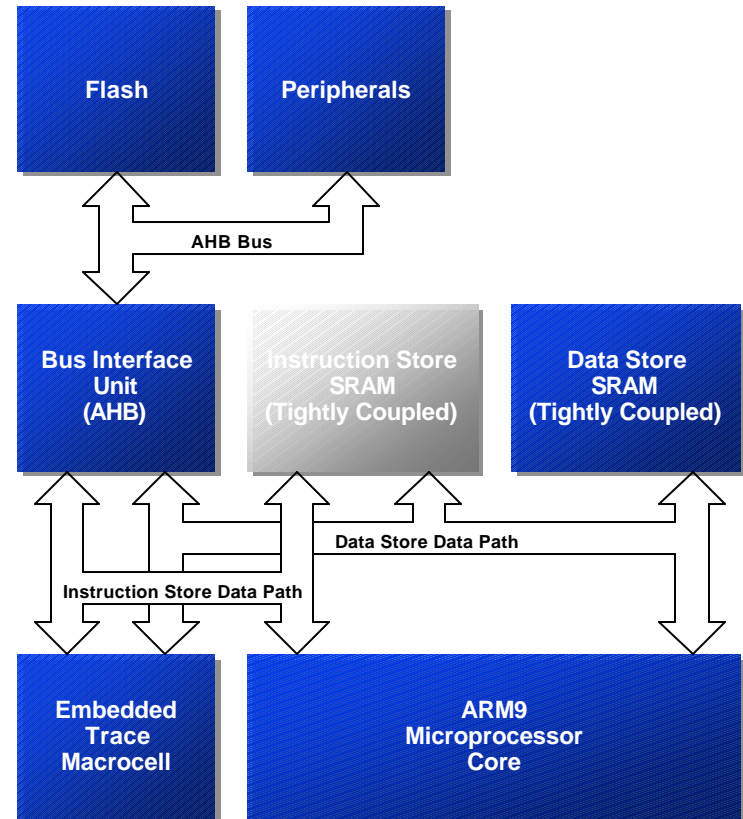
# Memory Architecture Alternative #3 “External Flash”

- **External Flash Advantages**

- Lowest Cost (No Duplication of Memory for Instruction Store)
- Ease of Programming (All Routines Execute at Same Speed, No Memory Partitioning)

- **External Flash Disadvantages**

- Lowest Performance (Stall Instruction Fetch On Data Access from Peripherals, Von Neumann Architecture)



# Memory Architecture Alternative #4

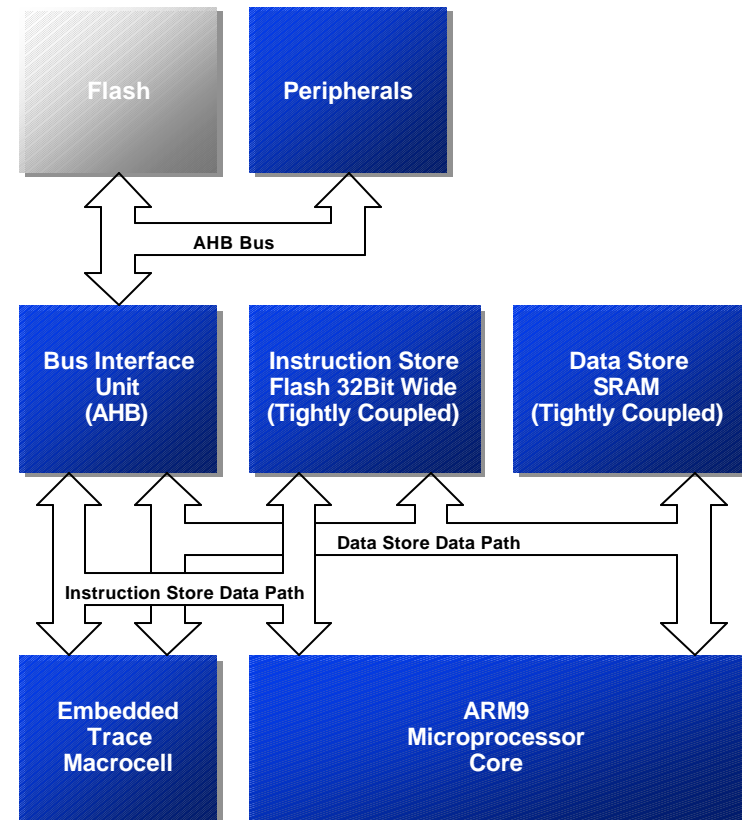
## *“Tightly Coupled Flash”*

- ***Tightly Coupled Flash Advantages***

- Higher Performance than *“Pseudo Cache”* (All Routines in Tightly Coupled Flash, Harvard Architecture)
- Ease of Programming (All Routines Execute at Same Speed, No Memory Partitioning)
- Lowest Cost (No Duplication of Memory for Instruction Store)

- ***Tightly Coupled Flash Disadvantages***

- Lower Performance than *“Enhanced Tightly Coupled Flash”* (Limited by Flash Access Time 20ns, Processor Limited to 50MHz)



# Memory Architecture Alternative #5

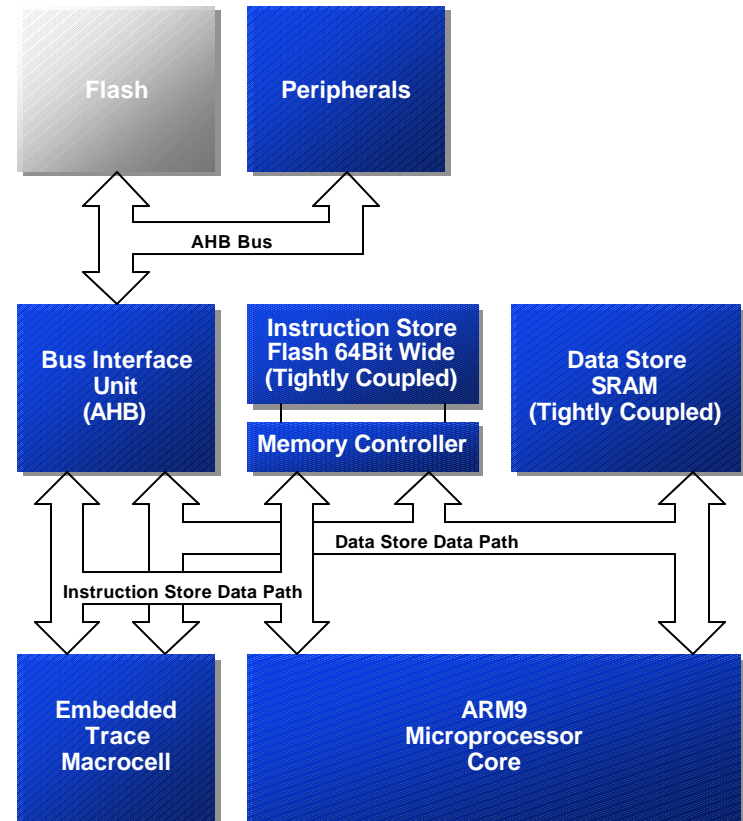
## *“Enhanced Tightly Coupled Flash”*

- ***Enhanced Tightly Coupled Flash Advantages***

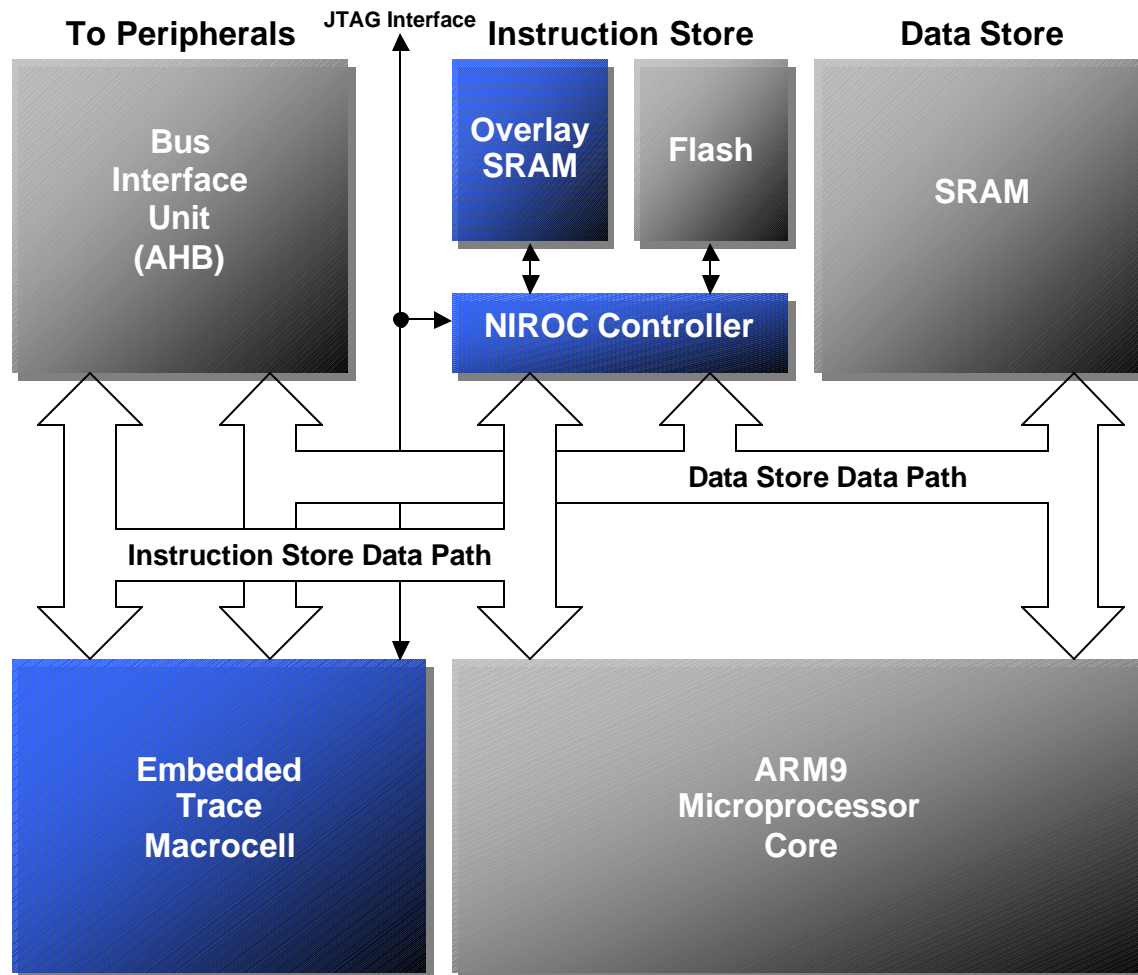
- Highest Performance (Wider Data Path Fetches 2 Instructions, Processor Runs at 100MHZ)
- Ease of Programming (All Routines Execute at Same Speed, No Memory Partitioning)
- Lowest Cost (No Duplication of Memory for Instruction Store)
- Expandability to > 64 Bits

- ***Enhanced Tightly Coupled Flash Disadvantages***

- Single Clock Stall On Branch



# Non-Intrusive RAM Overlay Calibration (NIROC)



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# Non-Intrusive RAM Overlay Calibration Strategy

- **Monitor Feedback Variables**
  - Embedded Trace Macrocell Automatically Monitors Control and Result Variables (Completely Non-Intrusive)
- **Copy Calibration Data to RAM Overlay**
  - Multi-ICE Tool Downloads Calibration Data through JTAG Port to NIROC Controller
  - NIROC Controller Loads RAM Overlay Independent of Microprocessor Flash Accesses (Completely Non-Intrusive)
- **RAM Overlay Enabled**
  - Multi-ICE Tool Downloads Command through JTAG Port to Enable RAM Overlay for Instantaneous Bank Switching of Coherent Data
  - NIROC Intercepts Microprocessor Calibration Data Accesses from Flash and Stuffs RAM Overlay Data to Microprocessor Bus
- **Instruction Store Re-Flashed with New Calibration Data**
  - Existing Flashing Routines Used to Re-Flash Instruction Store

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# Non-Intrusive RAM Overlay Specification

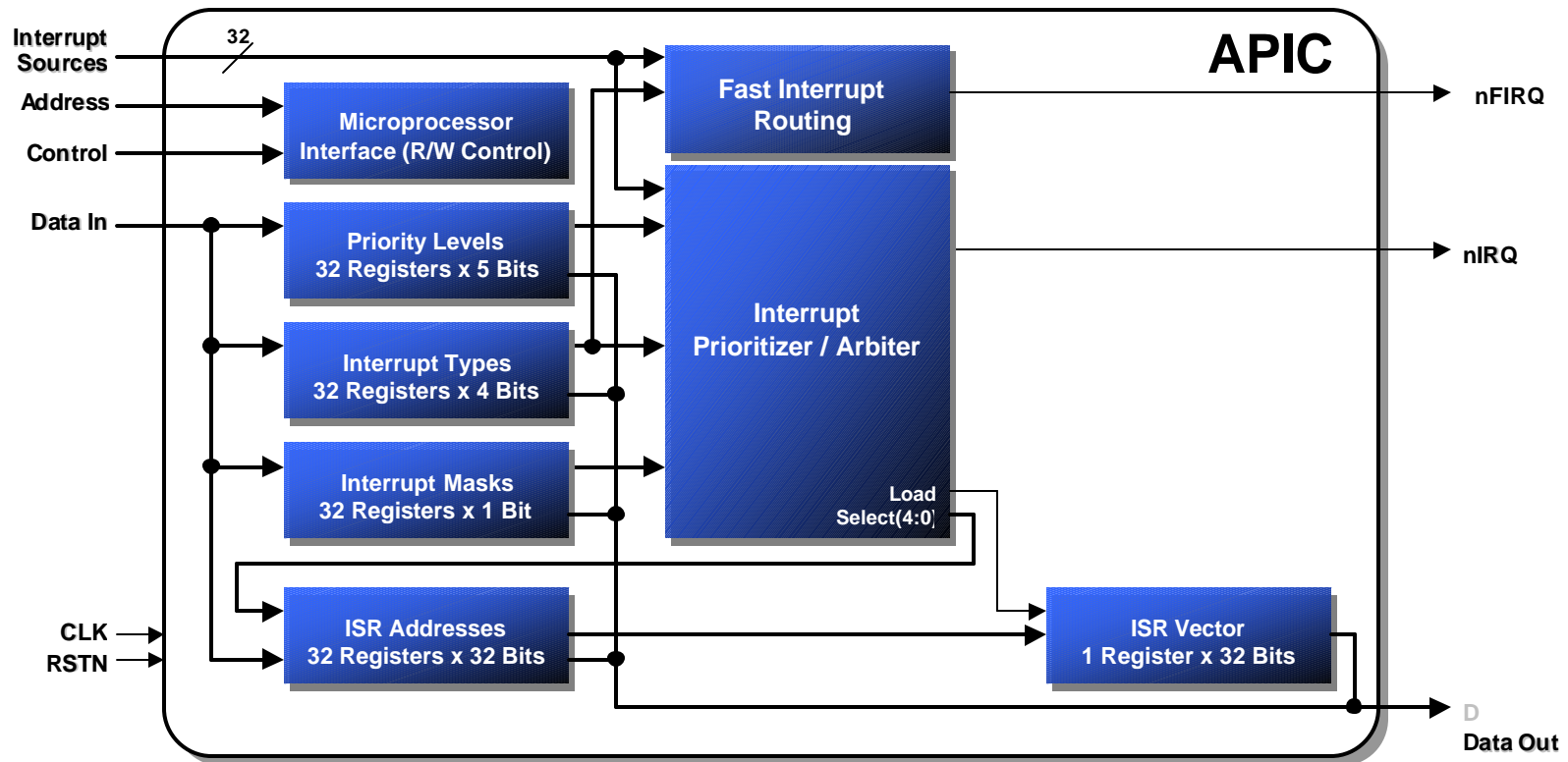
- **RAM Overlay for Modification of Calibration Data**
  - Writeable Via JTAG Interface (Non-Intrusive)
  - Writeable Via Microprocessor Core (Support Legacy Serial Port Calibration)
  - 2K x 32bits (8K Bytes)
  - 16 RAM Overlay Segments at 128 x 32bits (512 Bytes Each)
  - Instantaneous Bank Switching of Overlay Segments – Can Be Controlled by Application Software to Be Position Synchronous
- **Embedded Trace Macrocell for Monitoring of Feedback Variables**
  - Monitor of 16 Individual Variables or 8 Address Ranges of Variables or Any Combination Thereof
  - Application Software Controls Trace Updates of Variables Which Can Be Asynchronous, Time Synchronous, Or Position Synchronous
- **Rapid Prototype Development**
  - ASCET Support

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# ARM Processor Interrupt Controller Block Diagram



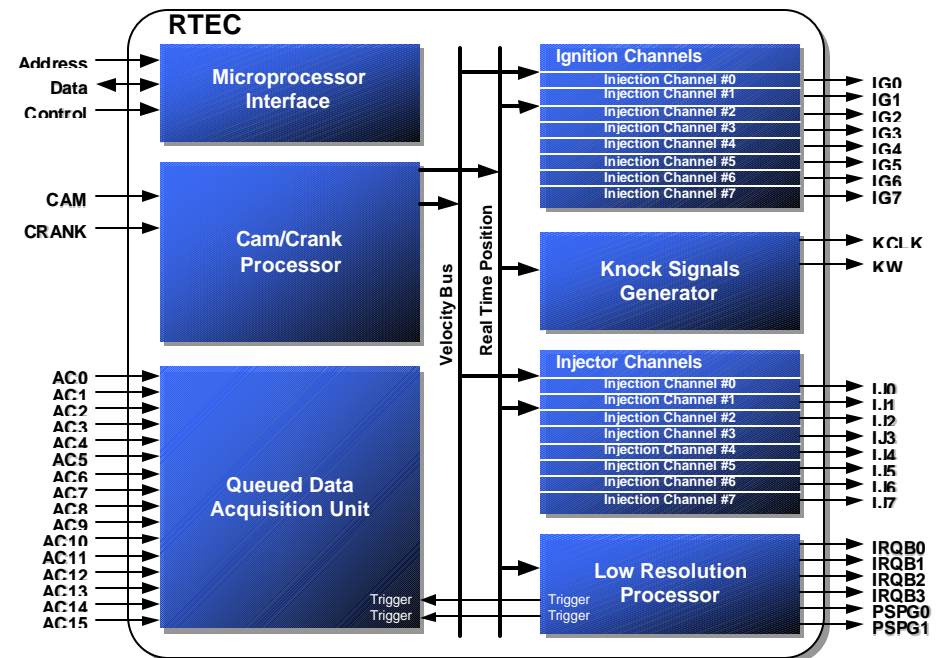
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# ARM Processor Interrupt Controller Features

- Compatible with ARM7TDMI and ARM9TDMI microprocessor cores
- Supports thirty-two interrupt sources for the nIRQ interrupt
- Any interrupt source can be routed to the nFIRQ interrupt
- Hardware interrupt vectoring reduces interrupt service routine latency
- Full hardware prioritization of interrupt sources
- Interrupts of lower priority levels automatically masked while interrupt is serviced
- Round-robin arbitration for interrupts at the same priority level ensures starvation-free operation under the heaviest of loading conditions
- Interrupt sources programmable with unique interrupt service routine addresses
- Thirty-two priority levels, programmable for each interrupt source
- Interrupts can have either a software or hardware source, Hardware interrupts can be active high or low, and edge or level-sensitive
- Masking programmable on a per-interrupt source basis

# Real Time Engine Controller (RTEC) Block Diagram

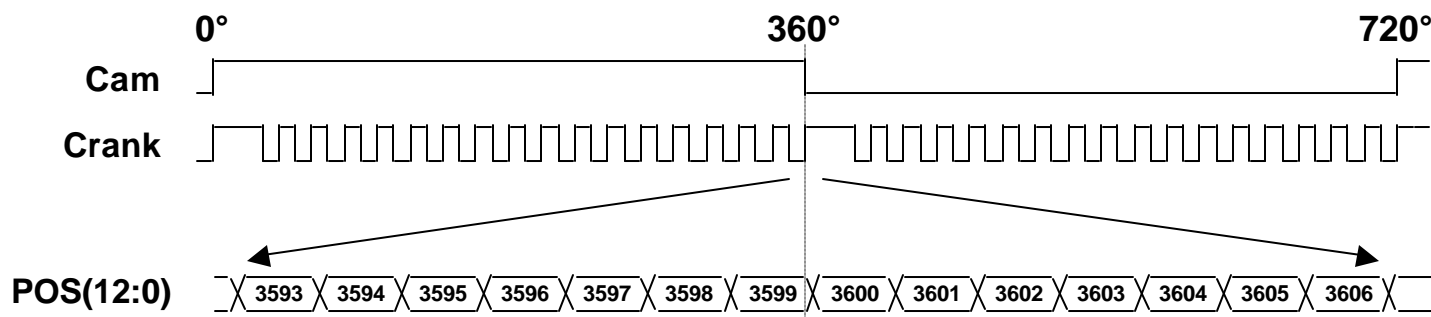
- **Cam / Crank Processor**
  - Accepts Arbitrary Tooth Patterns
  - Extremely Fast Lock Time
  - Cam Only Limp Home
  - Runs Completely Independent of uP
- **Ignition Channels / Knock Signals**
  - Wired OR Outputs Support Virtually all Ignition Strategies
  - Two uP Writes Control Ignition Sequence
  - Knock Signal Generation Independent of uP
- **Injection Channels**
  - Flexible 3 Pulse/Cycle Generation
  - Single uP Write Controls Injection Sequence
- **Low Resolution Processor**
  - Automatic Triggering of A-to-D
  - Precision Timing (Misfire Detection)
- **Queued Data Acquisition Unit**
  - 5 Independent Triggers (2 Position, 2 Time Based, 1 Software)
  - Queue Depth User Selectable



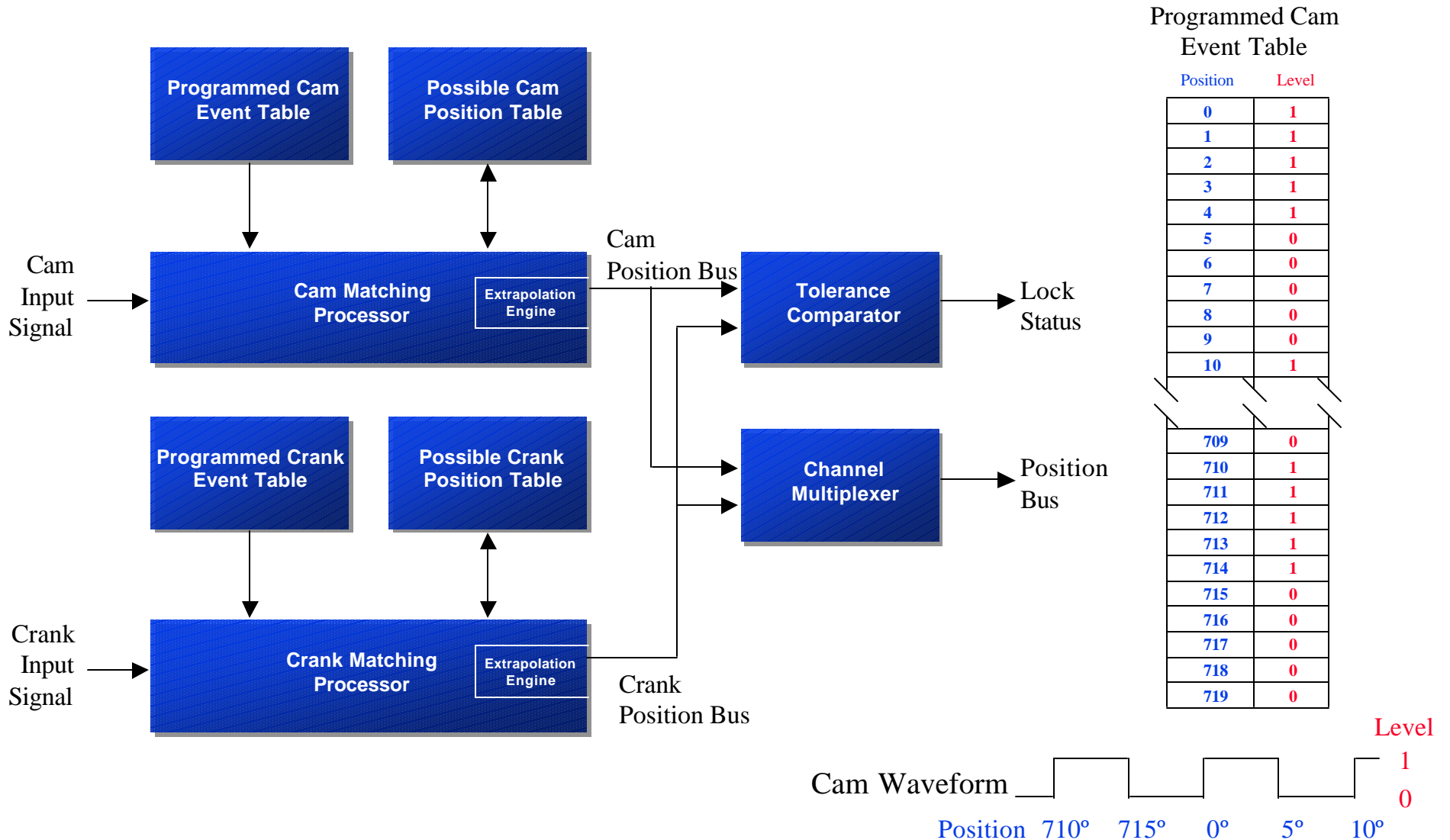
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# Cam / Crank Processor Module (CCPM) Functionality

- **Angular Position Tracking**
  - Angular Position Tracked Without Microprocessor Intervention
  - Real Time Position Bus (Range = 0.0°-719.9°, Resolution = 0.1°)
- **Independent Cam and Crank Channels**
  - Position Extrapolation On Cam Only or Crank Only Input Signals
- **Arbitrary Cam and Crank Waveforms**
  - Simple Configuration Through Table Programming



# Cam / Crank Processor Module (CCPM) Block Diagram



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# RTEC Data Acquisition Module (DAQM) Functionality

- **Automatically Acquires Analog Signals**

- Once Initialized, Requires No Further Microprocessor Intervention for Signal Acquisition

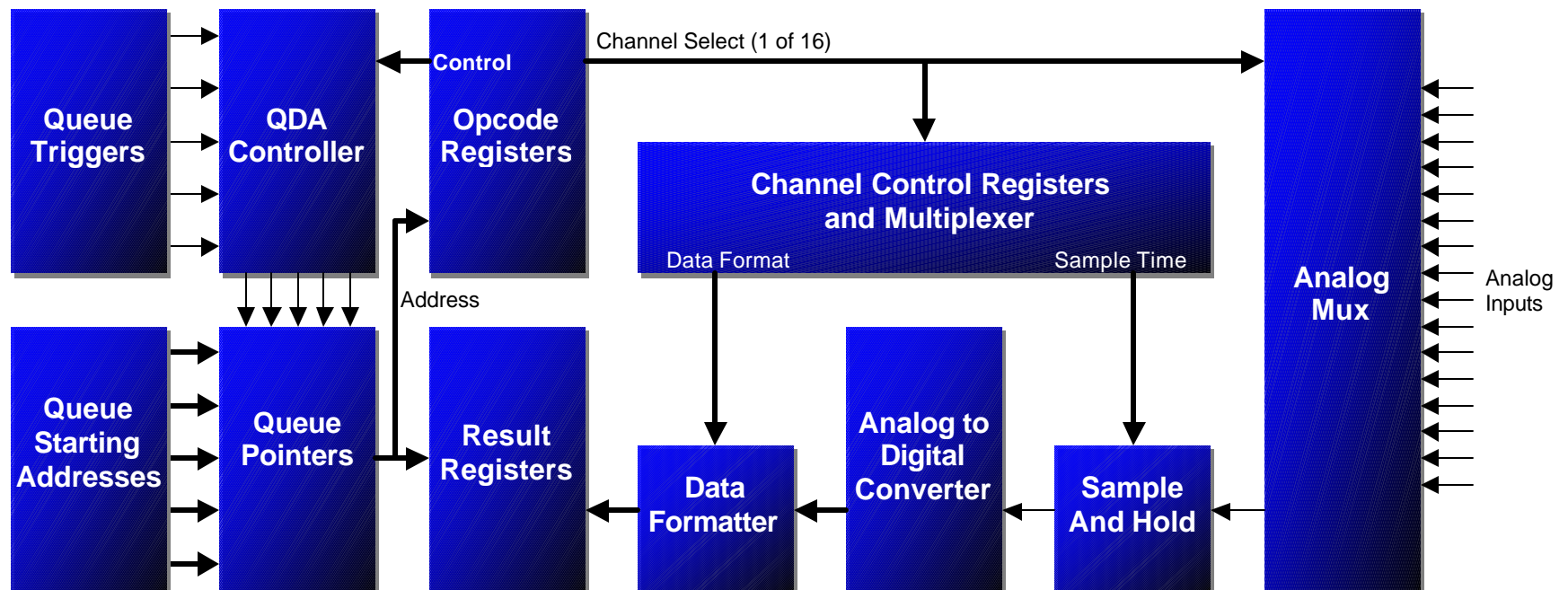
- **Analog to Digital Conversion - Position, Time and Software Triggered**

- 2 Independent Position Queues from 1 to 64 Acquisitions
- 2 Independent Time Based Queues with Programmable Intervals
- 1 Software Triggered Queue for On Demand Data Acquisition

- **Analog to Digital Converter Specifications (-40° to 125°, ±10% Supply)**

- 16 Channels, 10-Bit Resolution, ±1/2 LSB Accuracy
- 5µS Conversion Time, Guaranteed Monotonicity and No Missing Codes

# RTEC Data Acquisition Module (DAQM) Block Diagram

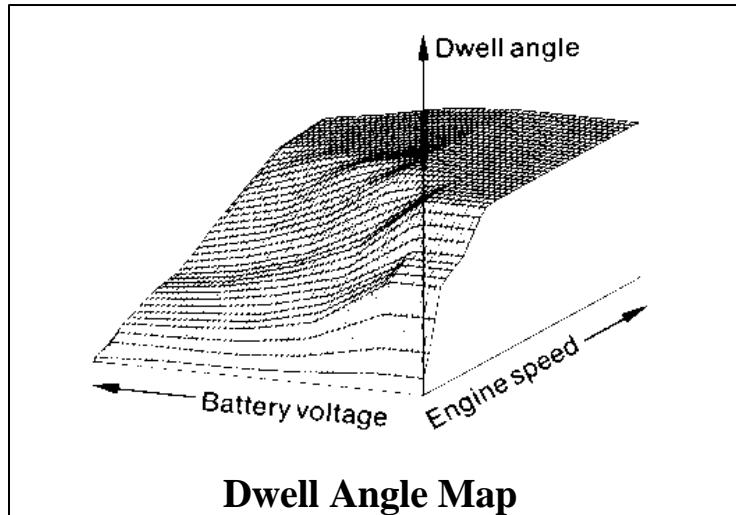


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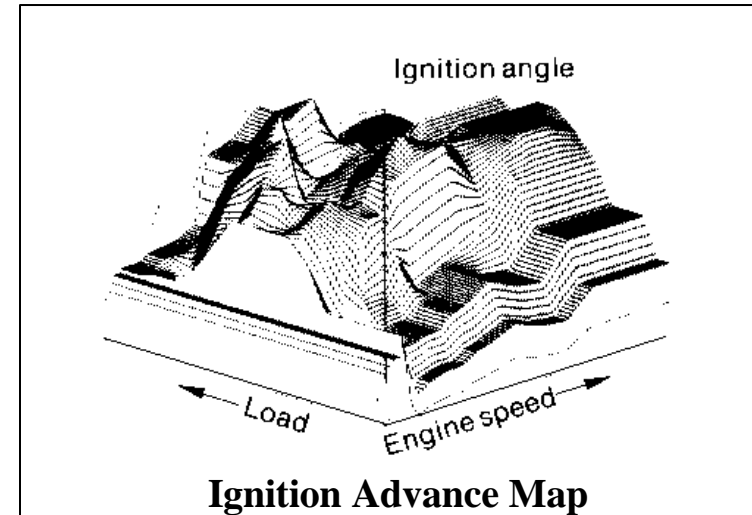
# RTEC Ignition Channel Module (IGCM) Functionality

- **Precision Ignition Timing**
  - 30uS Resolution Dwell Time Over Entire Operating Range (>500RPM)
  - 0.1° Resolution Ignition Advance Angle
- **Simplified Programming**
  - Single Write to Program Dwell Time
  - Single Write to Program Ignition Advance Angle
  - Ignition Channel Continues Without uP Intervention
  - Dwell Time and Advance Angles Programmed Synchronous or Asynchronous to Engine Events
- **Increased Performance**
  - Real Time Ignition Timing Per Spark for Increased Fuel Economy and Reduced Emissions

# Ignition Programming (Dwell and Ignition Advance Angles)



Robert Bosch GmbH, Automotive Electric/Electronic Systems



Robert Bosch GmbH, Automotive Electric/Electronic Systems

## Dwell Angle Programming

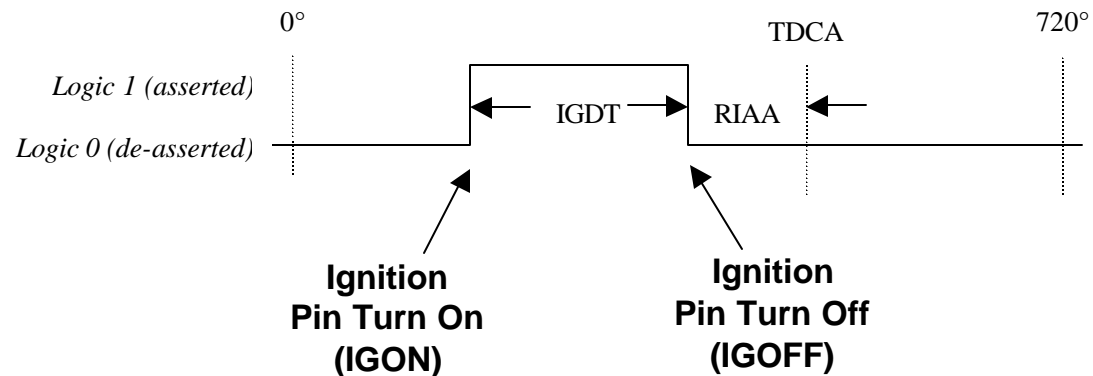
- 1) Read Battery Voltage from DAQM
- 2) Read Engine Velocity from CCPM
- 3) Fetch Dwell Angle from Map
- 4) Write Relative Dwell Angle to IGCM

## Ignition Advance Programming

- 1) Read Manifold Pressure from DAQM
- 2) Read Engine Velocity from CCPM
- 3) Fetch Ignition Advance from Map
- 4) Write Ignition Advance Angle to IGCM

- **Total of 8 Operations for Ignition Programming of a Cylinder**

# RTEC Ignition Channel Output Waveform



$IGOFF = TDCA - RIAA$

$IGON = IGOFF - (IGDT * Velocity)$

**TDCA - Top Dead Centers for Each Ignition Channel are Programmed Immediately after RESET**

**RIAA - Relative Ignition Advance Angle Programming Changes Take Effect Immediately**

**IGDT - Ignition Dwell Times Programming Changes Take Effect Immediately**

---

# RTEC Injector Channel Module (IJCM) Functionality

- **Precision Fuel Metering**

- 4uS Resolution Injector On Time Over Entire Operating Range (>500RPM)
- 0.1° Resolution Injector On/Off Angle

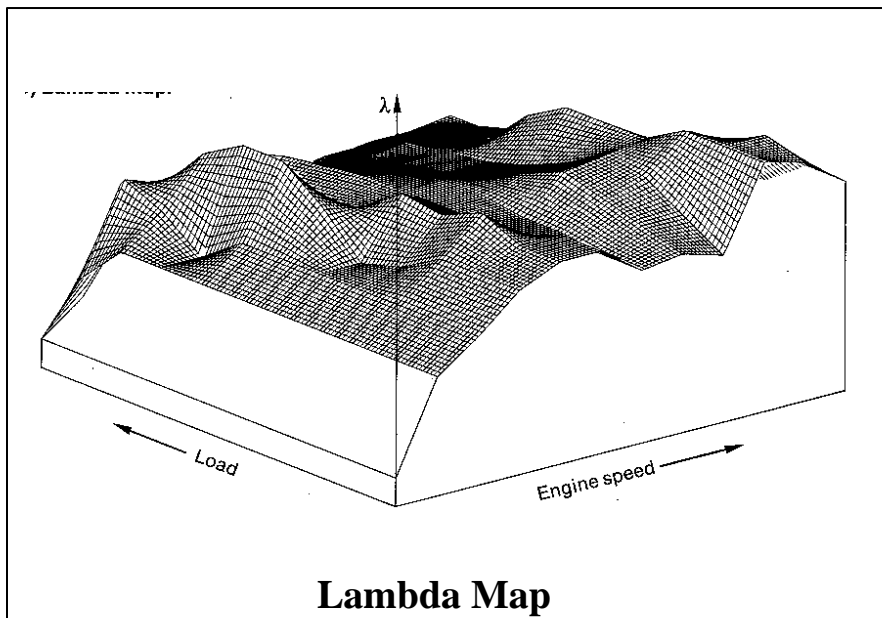
- **Simplified Programming**

- Single Write Instruction for Programming Total Commanded Pulse Width
- Injector Channel Continues Without uP Intervention
- Total Commanded Pulse Width Programmed Synchronous or Asynchronous to Engine Events

- **Increased Performance**

- Real Time Injector Timing Per Combustion for Increased Fuel Economy and Reduced Emissions

# Injector Programming (On Angle and Duration)

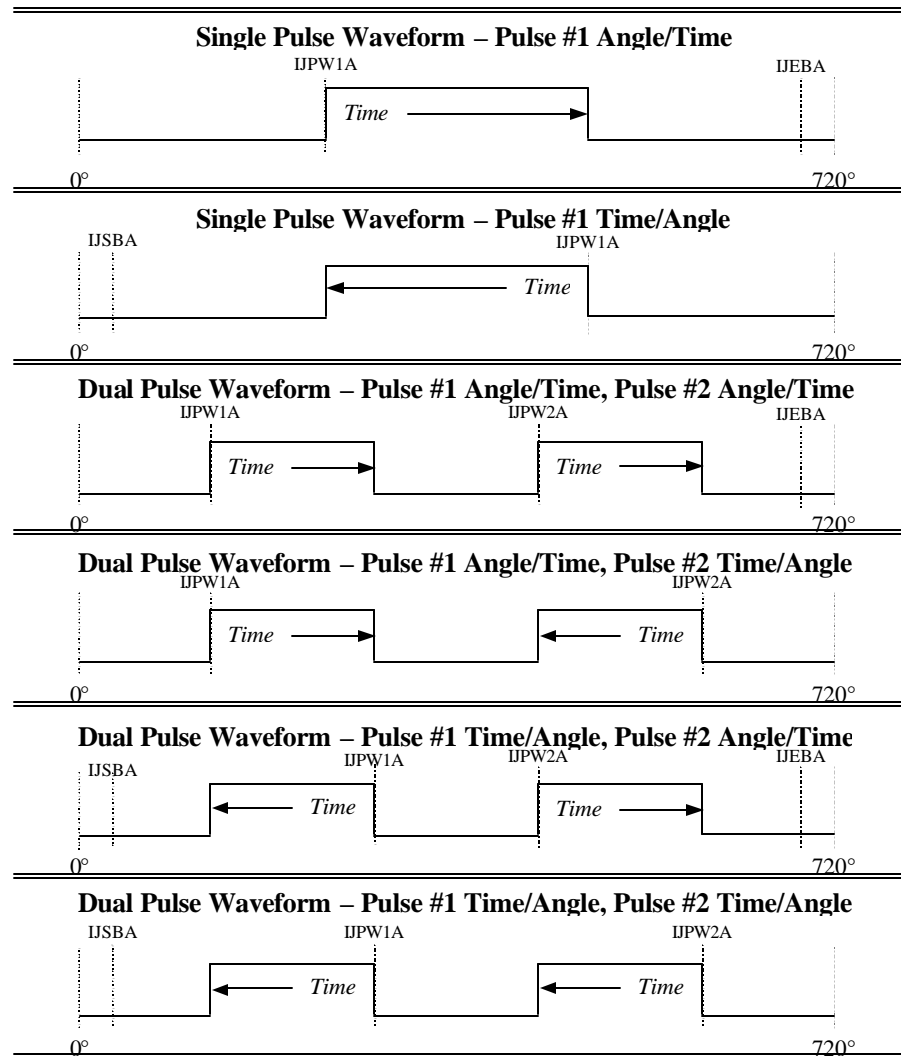


Robert Bosch GmbH, *Automotive Electric/Electronic Systems*

## Injector Programming

- 1) Read Manifold Absolute Pressure from DAQM
- 2) Read Engine Velocity From CCPM
- 3) Fetch Air/Fuel Ratio (Lambda) from Map
- 4) Read Mass Air Flow from DAQM
- 5) Read Battery Voltage from DAQM
- 6) Read Engine Temperature from DAQM
- 7) Read Air Temperature From DAQM
- 8) Read O<sub>2</sub> Sensor from DAQM
- 9) Read Throttle Valve Angle from DAQM
- 10) Read Throttle Valve Position from GPIO
- 11) Calculate Injector Period
- 12) Write Injector Total Commanded Pulse Width

# RTEC Injector Channel Module (IJCM) Output Waveform

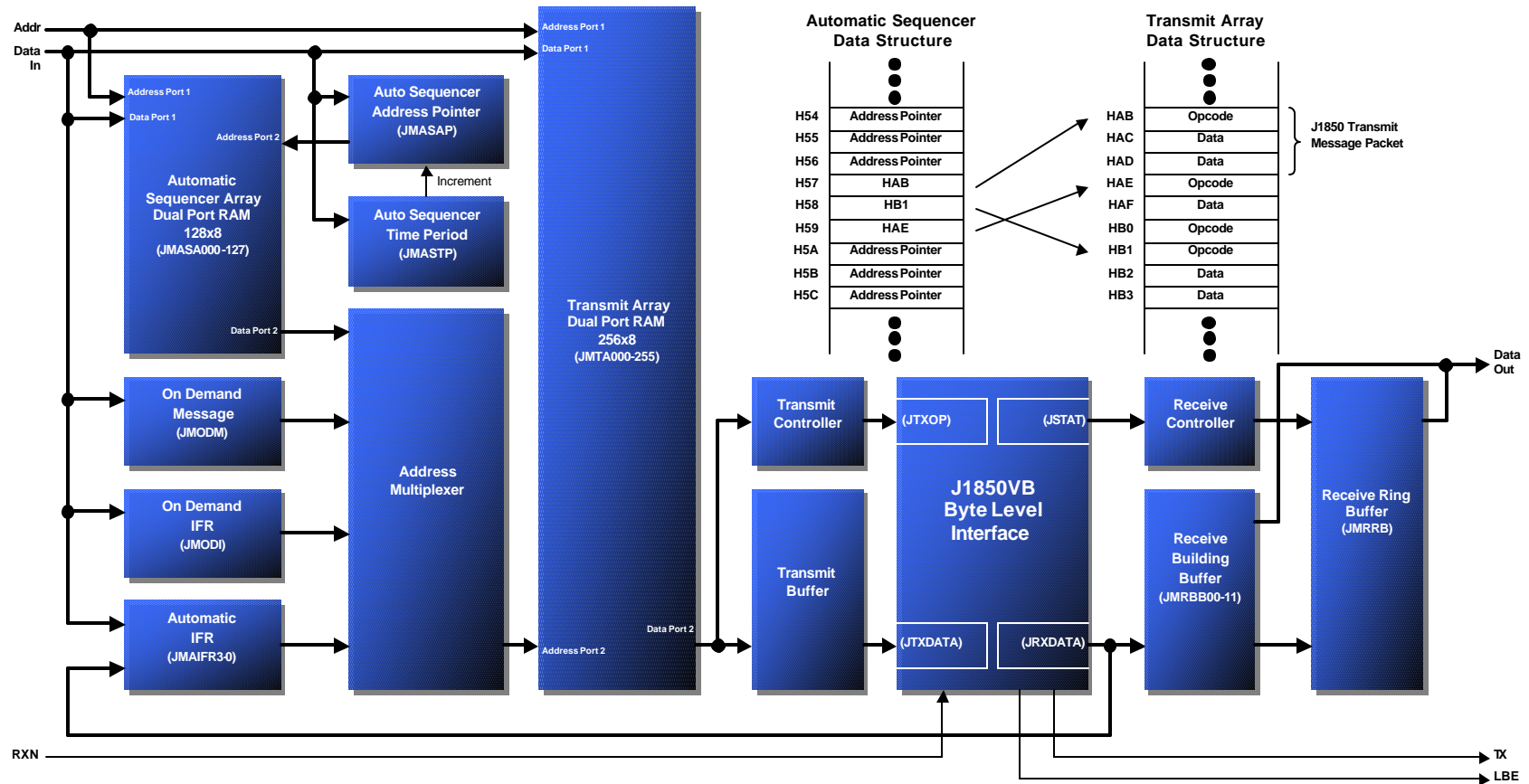


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# Communication Peripherals

- **Serial Communication Interface (SCI)**
- **Queued Serial Communication Interface (QSCI)**
- **Serial Peripheral Interface (SPI)**
- **Control Area Network (CAN)**
- **Variable Pulse Width Modulated Byte Level J1850**
- **Variable Pulse Width Modulated Message Level J1850**

# Message Level J1850 Block Diagram



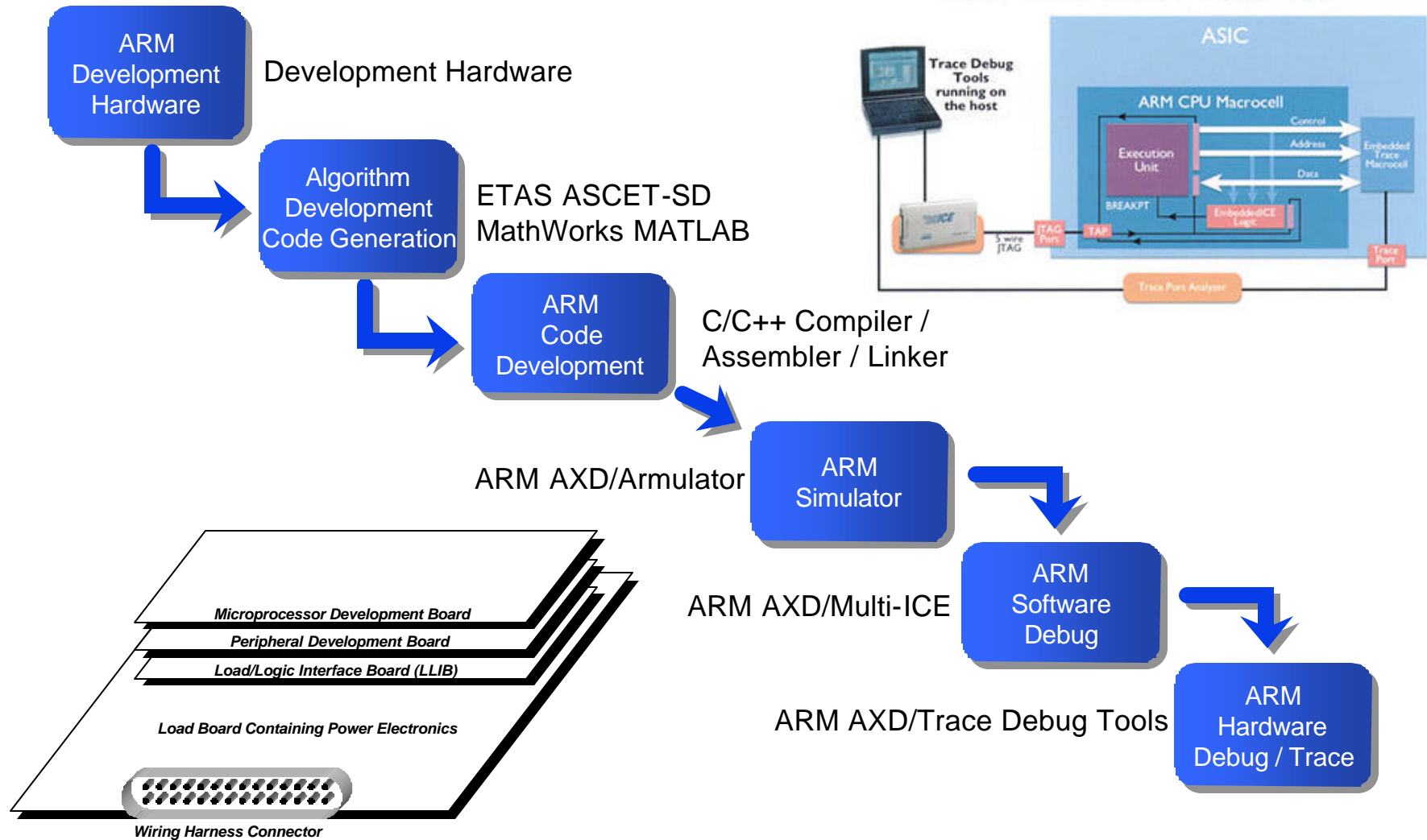
- Interrupt Free Transmission (No Microprocessor Intervention Required)
- Reduced Interrupt Reception (Message Filtering)
- Automatic In Frame Response (No Microprocessor Intervention Required)

---

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  - ✓ **Development Environment and Hardware**

# System Integration Development Environment



# Current System On Chip Development Platform

- **Microprocessor Development Boards**

- ✓ Includes Microprocessor Cores: ARM7, ARM9, ARM10
- ✓ Includes All Memory (Code and Data Store)
- ✓ Includes Advanced High Performance Bus Interface (AHB)

- **Peripheral Development Board**

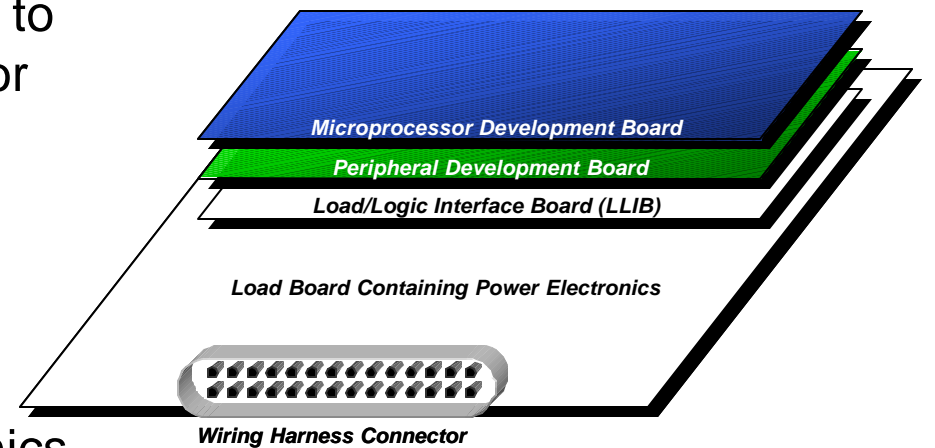
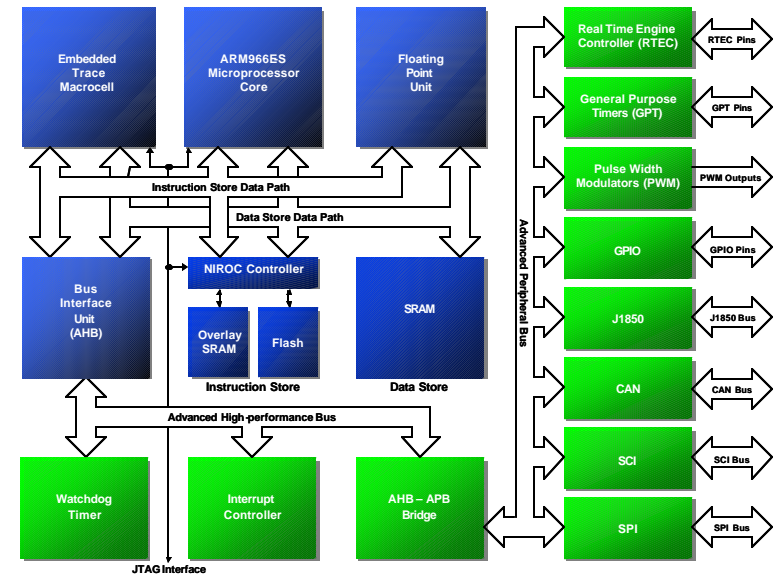
- ✓ All AIEC Peripherals Designed Using HDL (Verilog)
  - HDL Allows Targeting Peripherals to Virtually any Technology (FPGA for Prototyping, Standard Cell for Production)

- **Load/Logic Interface Board**

- ✓ A-to-D, Digital Level Shifting

- **Load Board**

- ✓ Customer Specific Power Electronics



---

# Current System On Chip Development Platform

- **System Hardware and Software Limited by 25MHz Clock Speeds and Memory Access Wait States**
- **Platform Does Not Support In System Calibration As Proposed Using NIROC/ETM/JTAG**
- **Platform Does Not Support Rapid Prototype Development As Proposed Using NIROC/ETM/JTAG**
- **Platform Supports Co-Design (Hardware/Software) Although Limited by Clock Speeds**
- **Development Platform Nearly Compatible with Production Intent Silicon**

# Future System On Chip Development Platform

- **uP / Peripheral Development Boards**

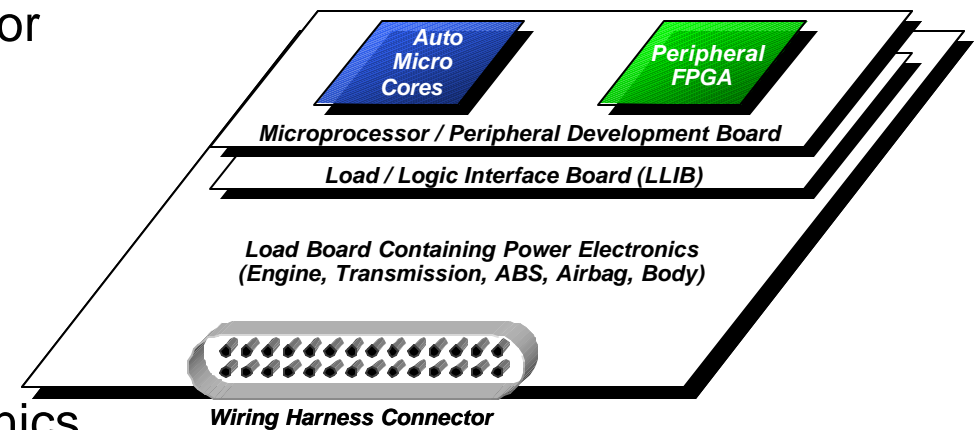
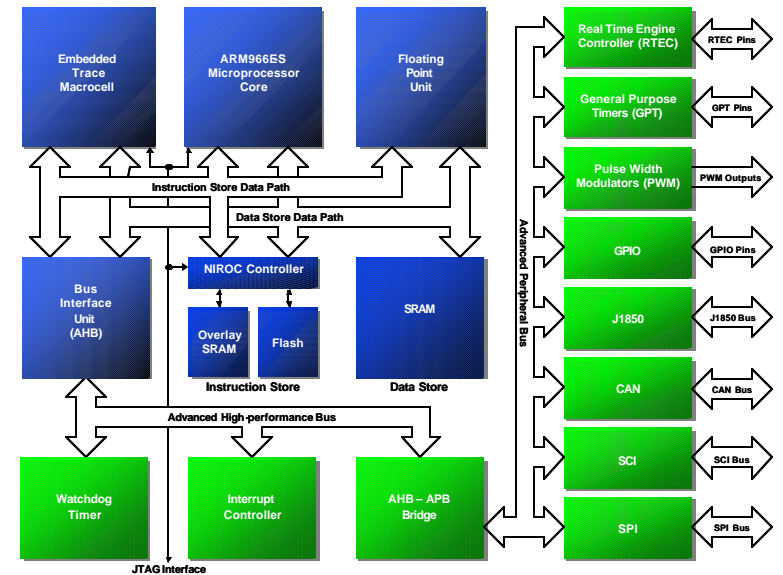
- ✓ Includes Microprocessor Cores: ARM7, ARM9, ARM10
- ✓ Includes All Memory (Code and Data Store)
- ✓ Includes Advanced High Performance Bus Interface (AHB)
- ✓ All AIEC Peripherals Designed Using HDL (Verilog)
- ✓ HDL Allows Targeting Peripherals to Virtually any Technology (FPGA for Prototyping, Standard Cell for Production)

- **Load/Logic Interface Board**

- ✓ A-to-D, Digital Level Shifting

- **Load Board**

- ✓ Customer Specific Power Electronics



---

# Future System On Chip Development Platform

- **System Hardware and Software Run at Targeted Application Speed**
- **Platform Supports In System Calibration (NIROC / ETM / JTAG Fully NEXUS Compliant)**
- **Platform Supports Rapid Prototype Development (NIROC / ETM / JTAG)**
- **Platform Supports Co-Design (Hardware/Software)**
- **Prototype Entire System before Committing to Silicon**
- **Development Platform Compatible with Production Intent Silicon**

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# Automotive System On Chip Summary

- **AIEC Develops Application-Specific System On Chip (SoC) Solutions for Automotive Industry**
- **SoC Allows Customer to Differentiate Product Over Standard Products through Higher Performance at Lower Cost**
- **AIEC Supports Industry-Standard ARM Microprocessor Cores; Broad Development Tool Support, Multiple Vendors**
- **There are Many Alternatives for Memory Architectures; AIEC Can Help Determine Which is Best For a Particular Application**
- **AIEC's NIROC Calibration Solution Supports Automotive Calibration Needs**
- **AIEC's Family of Intelligent Peripherals Offload Processor Bandwidth for Control Algorithm Processing**
- **AIEC's Development Systems Enable Rapid Development of Application-Specific SoC Solutions**